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THESIS

THE DESIGN, SIMULATION, AND FABRICATION OF A VLSI DIGITALLY PROGRAMMABLE GIC FILTER

by

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December 2000

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In this research, the design, simulation and mask layout for a VLSI Digitally Programmable Generalize Impedance Converter (GIC) Filter is presented. Programmable elements are filter type (low-pass, high-pass, band-pass and notch), center frequency and quality factor. The analog design eliminates the quantization errors, analog-to-digital and digital-to-analog conversion components, and the processing time delay associated with digital signal processing devices. Using a GIC as the basic circuit simplifies topology changes to realize the programmability function and eliminates a problematic component for integrated circuit fabrication, the inductor. Additionally, switched capacitor usage allows the elimination of resistors from the design, another problematic component for integrated circuits. The design was simulated with PSPICE while VLSI mask layout was performed with LASI. The chip has been submitted for fabrication to further research the design of analog VLSI circuits.

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THE DESIGN, SIMULATION, AND FABRICATION OF A VLSI DIGITALLY PROGRAMMABLE GIC FILTER

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EXECUTIVE SUMMARY

This thesis documents the design, simulation and mask layout of a VLSI Digitally Programmable Generalized Impedance Converter (GIC) Filter. This research enhances the ability to implement analog signal filtering in an integrated circuit (IC). The vast majority of current filtering functions are accomplished through Digital Signal Processing (DSP). DSP adds complexity to the filtering circuit by requiring analog-to-digital conversion, digital processing, and digital-to-analog conversion. A time delay is also introduced at each of these steps. Additionally, the analog-to-digital conversion introduces quantization errors. Using an analog filter can eliminate all of these disadvantages.

Analog filters have not been popular in integrated circuit form due to accuracy variation constraints found with some components. Inductors and resistors are inaccurate when made in IC form. Resistors can vary 50-100% from design. Since the filter center frequency is determined by the RC time constant, a variation of 50% in resistor value would cause a large variation in center frequency. This is unacceptable for reliable filtering. GIC topology is used to eliminate the need for inductors and allow simple programmability of filter function (low-pass, high-pass, band-pass or notch), center frequency and quality factor for the filter. GIC filters require very few components, and allow different functions with minor variations in component topology. Resistors are replaced with switched capacitor circuits to remove unacceptable variability brought about from using resistors. Using switched capacitors allows the center frequency to be determined from a ratio of capacitors in the circuit. This brings variation between different chips to 0.1% or less.

The filter was designed symbolically to provide the programmability of the four filter functions, eight selectable center frequencies within a frequency decade and six selectable quality factors. The decade of filtering is selected by the input clock frequency. Filtering decade is one decade below the clock decade. This design provides 192 different frequency responses per decade, up to 1 MHz, the design limit for this prototype chip. Greater frequency bandwidth is realizable if higher performance fabrication processes are used. The symbolic design was converted to a VLSI mask layout using LASI, a free for non-profit use layout program. The design was simulated in PSPICE, verifying proper filter operation. The chip design has been submitted to MOSIS for fabrication and will be available for further testing and research into analog VLSI devices.

I. INTRODUCTION

A. BACKGROUND

Filters are the backbone of many electronic systems. Electronic filters were first constructed out of passive elements such as resistors, capacitors, and inductors. They were complex, costly and sensitive to component variation. *Operational Amplifiers* (op amps) allowed the construction of active filters, which can eliminate a costly passive element, the inductor. With the advent of digital technology, systems that offered greater functionality appeared. *Digital Signal Processing* (DSP) is the focus for most systems requiring filtering functions and is the most commonly encountered solution for filtering needs. Despite the emergence and refinement of digital technology, the need for analog systems has not been removed. The world is experienced through analog signals. Our entire sensory system is constructed to process and interpret analog inputs. Thus, circuit designers must deal with analog signals in some fashion. Numerous electronic systems have analog input and output signals. All of these systems require analog-to-digital conversion prior to data processing and digital-to-analog conversion for output signals in order to take advantage of DSP. This conversion introduces additional equipment requirements, delayed circuit response, and quantization errors. Analog filters avoid the conversion errors, have less delay, and have reduced hardware requirements.

Digital systems have been preferred over analog systems due to the development of the *Integrated Circuit* (IC). Active analog systems required op-amps, resistors, and capacitors. Some of these elements are difficult to accurately produce in IC form, and require large areas of the chip. IC analog filters become attractive if these problematic components can be eliminated while maintaining necessary filter characteristics.

B. OBJECTIVE

The objective of the research is to develop an IC analog-analog filter design. The design needed to be accurately producible by modern IC fabrication techniques. Digitally programmability of various highly accurate filter specification functions is desired so the filter will easily interface with other digital systems either as a discrete component, or as part of a *System-on-a-Chip* design

C. RELATED WORK

Two previous theses have focused on the GIC filter. Ref. 7 developed the programmable aspects of this GIC filter, validated the design through breadboard tests, and demonstrated a basic, untested VLSI layout in Cadence. Ref. 6 further developed switched capacitor design theory, provided MATLAB frequency response charts of discrete-sized elements, and created modified layouts for filter subsections. This project furthers the GIC research by providing coverage of VLSI layout techniques, completing a new IC filter design in LASI, simulating the filter in PSPICE with correctly sized IC components, and submission of masks for production of test chips.

D. THESIS ORGANIZATION

Ch. II covers basic passive component filters. Ch. III introduces active filters and explores *the Generalized Impedance (or Immitance) Converter* (GIC) filter. Ch. IV explains switched capacitor resistor replacement. Ch. V covers VLSI design. Ch. VI symbolically develops a digitally programmable GIC filter. Ch. VII covers layout and filter simulation. Conclusions and recommendations for future work are discussed in Ch. VIII.

II. FILTERS

An electrical filter can be defined as an interconnected network of electrical components (resistors, capacitors, inductors, and transistors) that process applied electrical signals, referred to as *Input Signals* or *Excitations*. The result of processing performed by the network on an excitation is called an *Output Signal* or *Response*. The excitation and response differ according to the processing or filtering performed by the network. [Ref. 1] A filter is designed to provide *Frequency-Weighted* transmission. [Ref. 2] This frequency weighting attenuates portions of the signal's spectrum (stopbands) while passing or amplifying other portions (passbands). [Ref. 3] For example, we might want to amplify a weak audio signal with a large amount of noise. By attenuating the high frequency noise while amplifying the low frequency audio signal, a voice message could be understood.

A. FILTER TYPES

Filter design begins by specifying the transmission characteristics required for the filter. Generally, frequency selection is the basic design criteria. This involves passing signals whose frequency spectrum lies within a specified range, and stopping signals whose frequency spectrum falls outside this range. Ideally, the filter has frequency bands over which the magnitude of the transmission is unity (passband), and other frequency bands over which the transmission is zero (stopband). The ideal transmission characteristics of the four major filter types: *Low-Pass* (LP), *High-Pass* (HP), *Bandpass* (BP), and *Bandstop* (BS) (also known as *Band-Reject* or *Notch* (N)) are shown in Table 2.1. These idealized characteristics are known as *Brick-Wall* type responses because of their vertical edges. [Ref. 4]

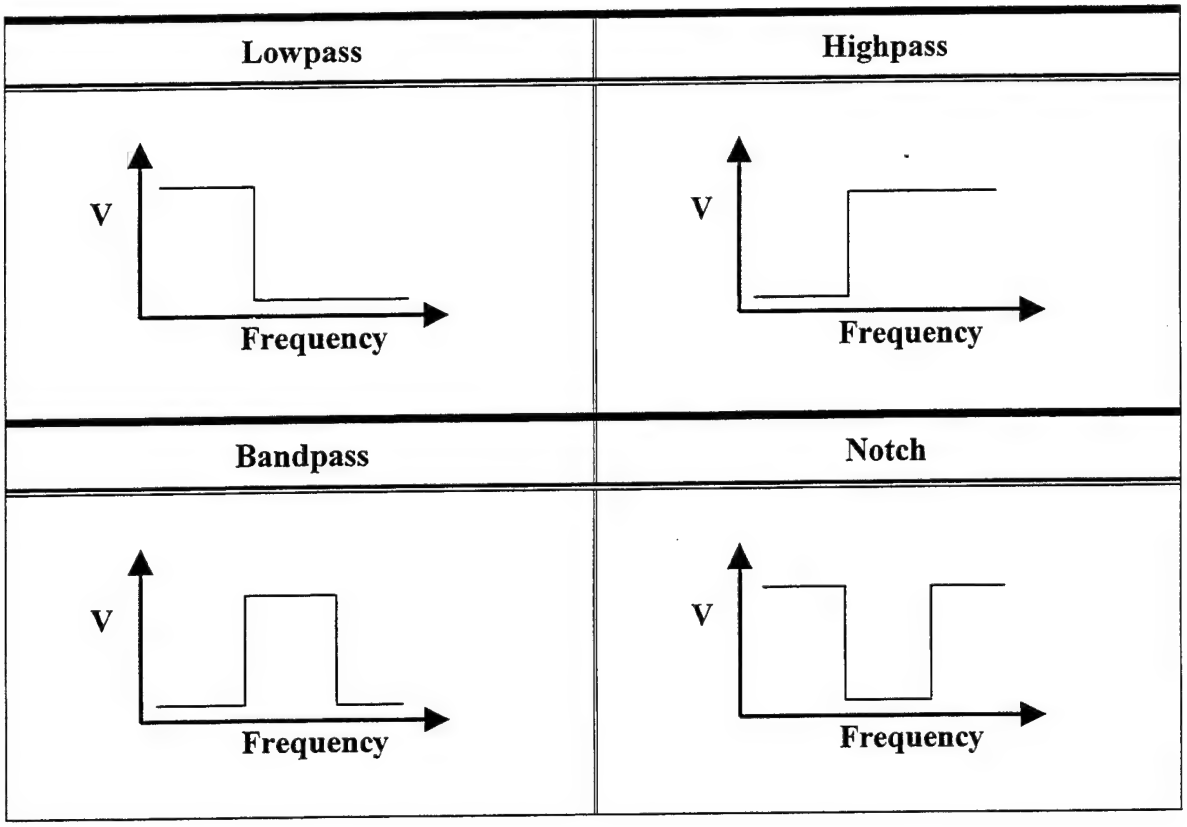


Table 2.1: Ideal Frequency Response of the Four Basic Filter Types. After Ref. [4]

Specifications for actual filters can not be given in the form shown in Table 2.1 because physical circuits cannot realize the brick-wall response. Physical filters demonstrate a transition band where the attenuation increases until it reaches the level of the stopband. This region extends from the edge of the passband (ω_p) to the edge of the stopband (ω_s).

The oldest type of physical technology for realizing filters makes use of inductors (L), capacitors (C), and resistors (R). [Ref. 4] Table 2.2 shows typical non-ideal frequency responses for the basic filter types using RLC filters. Additionally, simple RLC networks that provide the desired filter type are shown.

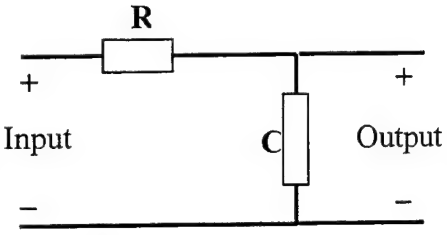
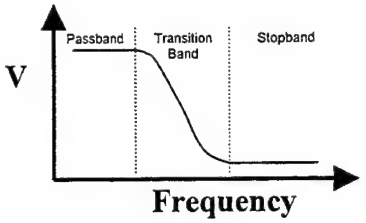
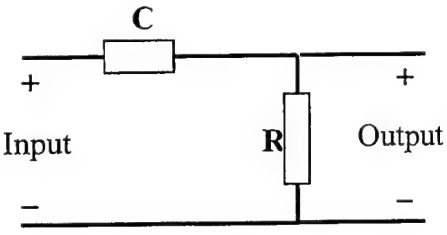
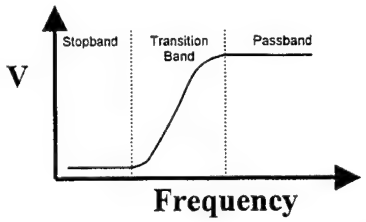
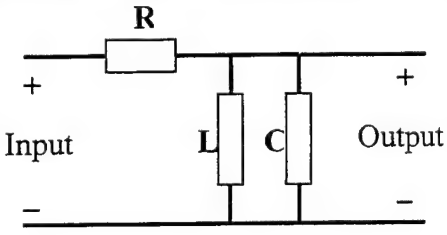
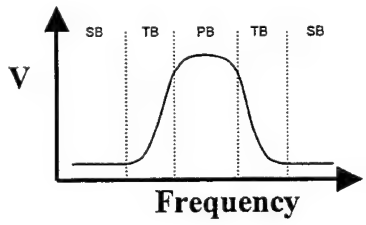
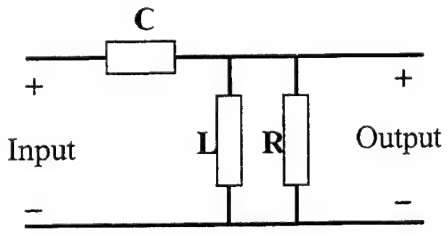
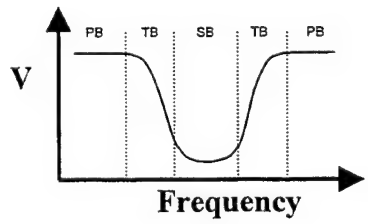
RC Low-Pass Filter	Non-Ideal Response
	
RC High-Pass Filter	**Non-Ideal Response**
	
RLC Band-Pass Filter	**Non-Ideal Response**
	
RLC Notch Filter	**Non-Ideal Response**
	

Table 2.2: Four Basic Filter Types with Corresponding Non-Ideal Frequency Responses. After Ref. [4]

Filter characteristics are specified using a mathematical model, the *Transfer Function*. The exponential degree of the denominator is known as the order of the filter. To achieve all basic filter types, the transfer function must be at least second order. Table 2.3 shows generalized transfer functions for each filter type. The center frequency is given by ω_p, while Q_p gives the quality factor, and a_i is a constant. [Ref. 4]

Filter Type	Transfer Function
Low-Pass	$T(s) = \dfrac{a_0}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
High-Pass	$T(s) = \dfrac{a_2 s^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
Band-Pass	$T(s) = \dfrac{a_1 s}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$
Notch	$T(s) = \dfrac{s^2 + \omega_p^2}{s^2 + \dfrac{\omega_p}{Q_p}s + \omega_p^2}$

Table 2.3: Transfer Functions of the Four Basic Filter Types. After Ref. [4]

B. FILTER SELECTIVITY

Since a physical circuit's transmission characteristics cannot change abruptly at the passband edge, a specification for the transition band characteristics must be established. The ratio of ω_s/ω_p is usually used as a measure of the sharpness of the filter

response and is called the *Selectivity Factor*. [Ref. 4] Another term used for the selectivity is the *Quality Factor* (Q). [Ref. 5] A filter exhibiting maximum frequency selectivity is usually desirable, because tighter specifications create a response closer to ideal. However, the resulting filter circuit will be higher order and more complex to implement. [Ref. 4]

For most filters the quality factor is an important parameter. It is especially important in band-pass filters, which are used to pass only a narrow band of frequencies. [Ref. 1] Figure 2.1 illustrates the quality factor for a band-pass filter.

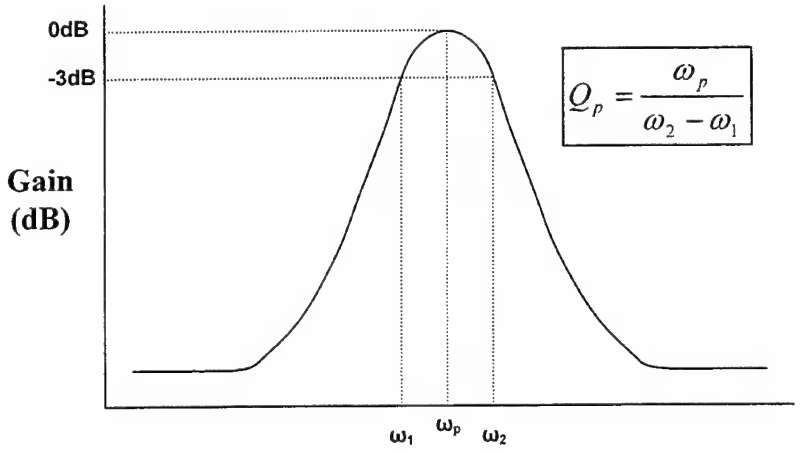


Figure 2.1: Q-Factor of Bandpass Filter. After Ref. [4]

The quality factor of a filter will often determine what applications it is appropriate for, and its general usefulness. Therefore, any filter design project must include a specification for the quality factor. [Ref. 6]

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III. GIC FILTERS

A. OPERATIONAL AMPLIFIERS

The op amp is a universally important building block for circuit designs in general, and to the GIC in particular. Early op amps were constructed using discrete components (vacuum tubes first, then transistors and resistors), and were prohibitively expensive (up to $1000 for a good discrete transistor op amp). The original IC op amp, the μA 709 became available in the mid-1960s. Although its quality was low compared to today's standards, and its price was still high, engineers began using them in large quantities. This accelerated the introduction of improved devices and drove the prices down (tens of cents). The op amp is popular due to its versatility. Many different types of electrical circuits can be created with an op amp. Another important factor for design is that IC op amps closely approach the assumed ideal. This makes it relatively easy to design circuits using IC op amps. [Ref. 4]

Despite this, there are several characteristics that limit performance to less than the ideal. In this project two important op amp limiting factors will be considered, operating frequency and output voltage swing.

1. Gain

The most common op amp configuration has five basic connections shown in

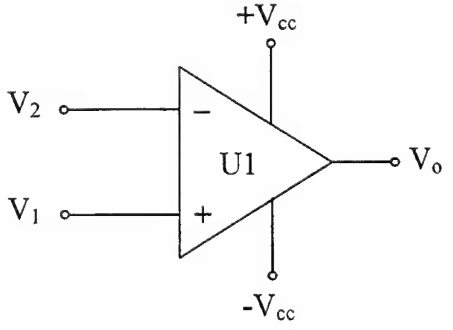

Figure 3.1: Op Amp Circuit Symbol. After Ref. [4]

Figure 3.1. Usually in schematic representations, the +Vcc and –Vcc connections are implied and thus cmitted. Open-loop gain is defined by the following equation.

$$V_o = A(V_1 - V_2) \Rightarrow A = \frac{V_o}{(V_1 - V_2)} \qquad \text{(Eq. 3.1)}$$

The ideal op amp has infinite gain. Using this approximation allows another approximation to be used that makes it easier to use the op amp, $V_1 = V_2$. Realizable op amps usually have a gain in the range of 100 to 10E6. [Ref. 6] The linear relationship between input and output voltage is only valid for a finite range inside the values of +Vcc and -Vcc. For example, the range for a μA 741 connected to +/–15 V is about –11 V to +12 V. This finite linear range is the maximum output voltage possible without signal clipping. [Ref. 7]

2. Bandwidth

The main limiting factor for an op amp is its frequency response. The ideal op amp has a constant gain across all frequencies, or infinite bandwidth. Realizable op amps do not have infinite bandwidth. Internal parasitic capacitance limits the bandwidth. To make op amps stable, designers usually include a compensating capacitor to set the first pole of the device. The position of this pole is selected to ensure the gain is less than one before the phase response inverts from the next parasitic pole, thus preventing positive feedback. Such *Internally Compensated* op amps usually show a uniform gain roll-off of -20dB/decade. Figure 3.3 shows a typical non-ideal frequency response of general op amps such as the μA 741. This finite bandwidth is the main limiting factor for maximum operating frequencies of a circuit utilizing op amps. [Ref. 6]

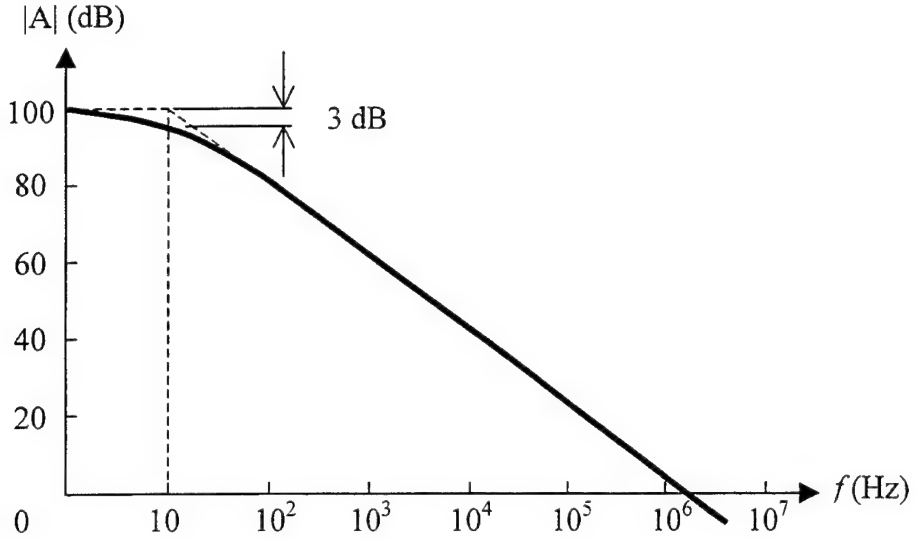

Figure 3.3: Typical Non-Ideal Op Amp Frequency Response. After Ref. [4]

3. Slew Rate

Another limitation on bandwidth is the *Slew Rate*. Op amps have a specific maximum rate of change possible at the output called slew rate. This is defined as

$$SR = \left.\frac{dV_o}{dt}\right|_{\max} \qquad \text{(Eq. 3.2)}$$

and is usually specified in units of V/μs. The slew rate can cause non-linear distortion to a signal when the frequency and amplitude would require an output change greater than the slew rate. This leads to a full-power bandwidth limitation derived as follows with a sinusoidal input.

$$v_i = \hat{V}_i \sin \omega t \qquad \text{(Eq. 3.3)}$$

The rate of change of the waveform is given by

$$\frac{dv_i}{dt} = \omega \hat{V}_i \cos \omega t \qquad \text{(Eq. 3.4)}$$

The maximum value occurs at

$$\left.\frac{dv_i}{dt}\right|_{\max} = \omega_m \hat{V}_i \qquad \text{(Eq. 3.5)}$$

Equating to slew rate and solving for the maximum frequency results in

$$f_M = \frac{SR}{2\pi \hat{V}_{O\max}} \qquad \text{(Eq. 3.6)}$$

Figure 3.4 shows slew rate distortion on a sinusoidal signal.

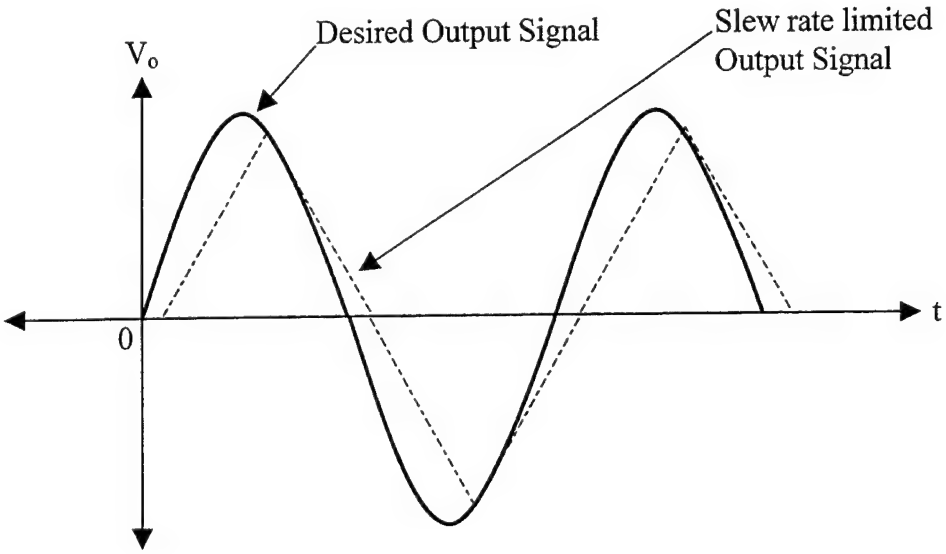

Figure 3.4: Slew Rate Limited Sinusoidal Signal. After Ref. [4]

Inspecting the maximum frequency Eq. 3.6 shows that output sinusoids with smaller output voltages will show slew rate distortions at frequencies higher than ω_M. [Ref. 4] Slew rate, along with high required output voltages, imposes a limitation on bandwidth. One way to avoid this limitation is to use small output signals. Finding a compromise of lower output voltage and desired signal-to-noise ratio is the key trade-off in this decision.

B. INDUCTOR SIMULATION

Resistors and inductors are two troubling components when implemented using IC techniques. Employing op amp circuits allows the elimination of inductors in network design by using inductor simulation techniques. There have been many op amp-RC circuits proposed to simulate inductor operation. The GIC circuit, invented by A. Antoniou in 1969, has proven to be the "best" over time. "Best" being defined as very tolerant of op amp non-ideal properties, in particular finite gain and bandwidth. [Ref. 4] Figure 3.5 shows the Antoniou GIC circuit.

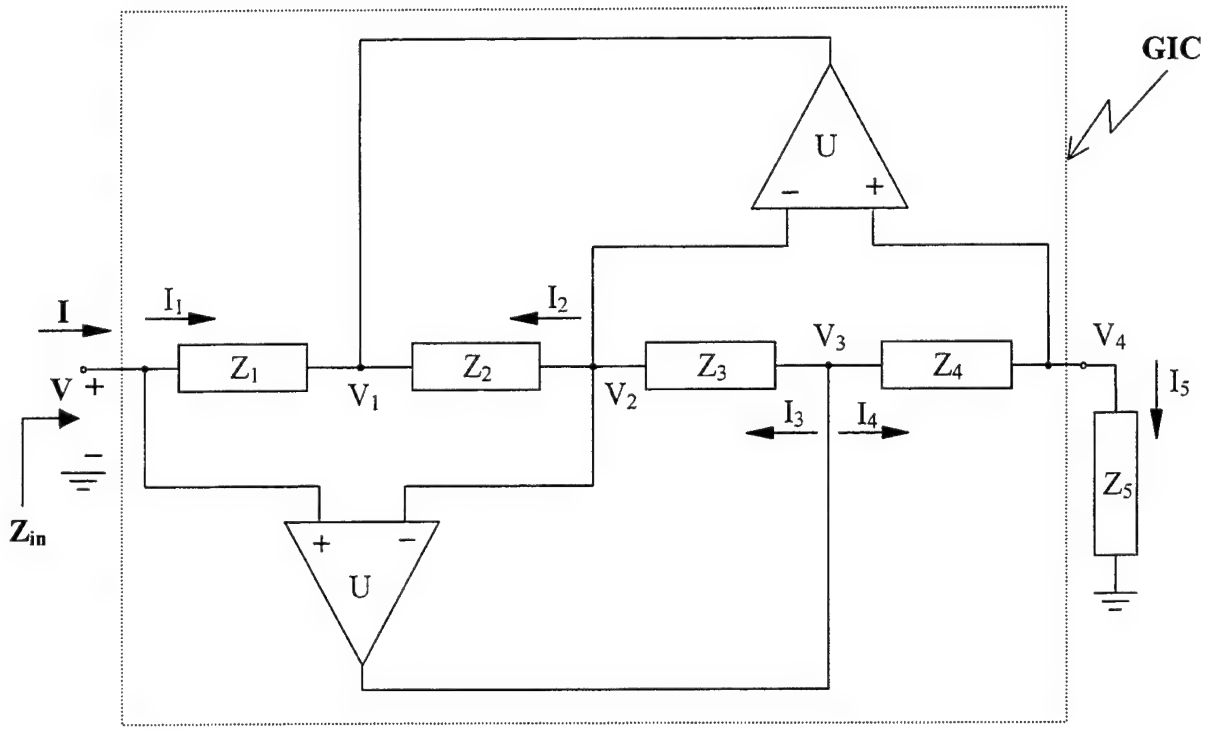

Figure 3.5: Op Amp Network for Inductor Simulation. After Ref. [2]

Using nodal analysis, it can be shown that the circuit in Figure 3.5 behaves as an inductor simulator. Input impedance is given by

$$Z_{in} = \frac{V}{I} \qquad \text{(Eq. 3.7)}$$

The current at the load is

$$I_5 = \frac{V_4}{Z_5} = \frac{V}{Z_5} \qquad \text{(Eq. 3.8)}$$

The second equality arises from a virtual short from input voltage to V_4. Noting input impedance of op amps is theoretically infinite, thus drawing no current

$$I_4 = I_5 = \frac{V}{Z_5} \qquad \text{(Eq. 3.9)}$$

The voltage at V_3 is given by

$$V_3 = V_4 + I_4 Z_4 \qquad \text{(Eq. 3.10)}$$

Substituting the value of I_4 from Eq. 3.9, and $V_4 = V$ due a virtual short

$$V_3 = \left(1 + \frac{Z_4}{Z_5}\right) V \qquad \text{(Eq. 3.11)}$$

Current I_3 is given by

$$I_3 = \frac{V_3 - V_2}{Z_3} = \frac{\left[\left(1 + \frac{Z_4}{Z_5}\right) V - V\right]}{Z_3} \qquad \text{(Eq. 3.12)}$$

Simplifying Eq. 3.12 provides

$$I_3 = \frac{Z_4}{Z_5} \frac{V}{Z_3} \qquad \text{(Eq. 3.13)}$$

Summing the currents at V_2, and assuming op amps draw negligible current

$$I_2 = I_3 \qquad \text{(Eq. 3.14)}$$

Voltage at V_1 is

$$V_1 = V_2 - I_2 Z_2 = V - I_3 Z_2 = V - V\frac{Z_4 Z_2}{Z_5 Z_3} \qquad \text{(Eq. 3.15)}$$

Current I_1 is

$$I_1 = \frac{V - V_1}{Z_1} = \frac{V - V + V\left(\frac{Z_2 Z_4}{Z_3 Z_5}\right)}{Z_1} = V\left(\frac{Z_2 Z_4}{Z_1 Z_3 Z_5}\right) \qquad \text{(Eq. 3.16)}$$

Noting $I = I_1$, the equation for the circuit's input impedance is

$$Z_{in} \equiv \frac{V}{I} = \frac{Z_1 Z_3}{Z_2 Z_4} Z_5 \qquad \text{(Eq. 3.17)}$$

This gives the general input impedance for the circuit in terms Z. By choosing the impedances properly, one can simulate an inductance. Choosing components

$$Z_1 = R_1, \quad Z_3 = R_3, \quad Z_4 = R_4, \quad Z_5 = R_5, \quad \text{and } Z_2 = \frac{1}{sC}$$

and substituting into Eq. 3.17 gives

$$Z_{in} = sC\frac{R_1 R_3 R_5}{R_4} \qquad \text{(Eq. 3.18)}$$

or

$$Z_{in} = sL, \quad \text{with } L = C\frac{R_1 R_3 R_5}{R_4} \qquad \text{(Eq. 3.19)}$$

The capacitor in the circuit acts as an inductor, with inductance value determined by the capacitor and resistor values used. [Ref. 2] By using this type of circuit, inductors can be eliminated from IC designs.

C. GIC FILTERS

The basic GIC circuit can be used to realize all filter types with only minor changes in components. The GIC filter design used in this project has proven to be highly insensitive to non-ideal component characteristics and variations in component values. [Ref. 2] By only requiring small changes in components to realize completely different filters, it is a good choice for a programmable device. Figure 3.6 shows the GIC filter circuit with general admittance values Y.

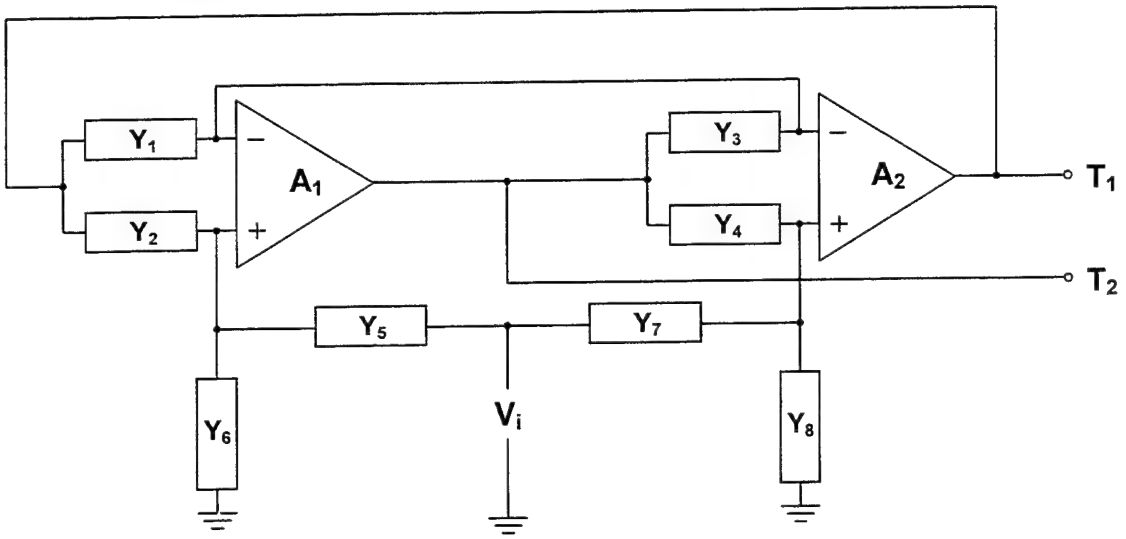

Figure 3.6: GIC Filter Circuit Network. After Ref [2]

S. Michael [Ref. 2] derived (derivation shown in [Ref. 6]) the transfer functions for output nodes T_1

(Eq. 3.20)

$$T_1 = \frac{V_1}{V_i} = \frac{Y_1Y_4Y_5 + Y_2Y_3Y_7 + Y_3Y_6Y_7 - Y_3Y_5Y_8}{Y_1Y_4Y_5 + Y_1Y_4Y_6 + Y_2Y_3Y_7 + Y_2Y_3Y_8} \quad \text{or} \quad T_1 = \frac{V_1}{V_i} = \frac{Y_1Y_4Y_5 + Y_3Y_7(Y_2 + Y_6) - Y_3Y_5Y_8}{Y_1Y_4(Y_5 + Y_6) + Y_2Y_3(Y_7 + Y_8)}$$

and T_2

(Eq. 3.21)

$$T_2 = \frac{V_2}{V_i} = \frac{Y_1Y_4Y_5 + Y_1Y_5Y_8 + Y_2Y_3Y_7 - Y_1Y_6Y_7}{Y_1Y_4Y_5 + Y_1Y_4Y_6 + Y_2Y_3Y_7 + Y_2Y_3Y_8} \quad \text{or} \quad T_2 = \frac{V_2}{V_i} = \frac{Y_1Y_4Y_5 + Y_1Y_5Y_8 + Y_2Y_3Y_7 - Y_1Y_6Y_7}{Y_1Y_4(Y_5 + Y_6) + Y_2Y_3(Y_7 + Y_8)}$$

By substituting resistors (G), capacitors (C), and open circuits (0) for the various admittances, all filter types may be realized. Table 3.1 shows components and output

Filter Type	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Transfer Function
Low-Pass	G	sC	$sC+\frac{G}{Q_p}$	G	G	0	0	G	$T_2=\frac{2\omega_p^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
High-Pass	G	G	sC	G	0	G	sC	$\frac{G}{Q_p}$	$T_1=\frac{2s^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
Band-Pass	G	G	sC	G	0	G	$\frac{G}{Q_p}$	sC	$T_1=\frac{2\frac{\omega_p}{Q_p}s}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
Notch	G	G	sC	G	G	0	sC	$\frac{G}{Q_p}$	$T_2=\frac{s^2+\omega_p^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$

Table 3.1: GIC Filter Admittance Values. After Ref. [2]

node to realize each filter type and shows the second order transfer function.

These transfer functions are based upon the use of ideal op amps. Non-ideal transfer functions S. Michael [Ref. 2] derived (derivation shown in [Ref. 6]) are shown below.

The non-ideal transfer function for T_1

(Eq. 3.22)

$$T_1=\frac{V_1}{V_i}=\frac{\frac{\left[Y_7(Y_1+Y_3)(Y_2+Y_5+Y_6)\right]}{\omega_{t_1}}s+\left[Y_1Y_4Y_5+Y_2Y_3Y_7+Y_3Y_6Y_7-Y_3Y_5Y_8\right]}{\frac{(Y_1+Y_3)(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}\omega_{t_2}}s^2+\frac{Y_1(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}}s+\frac{Y_3(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_2}}s+\left[Y_1Y_4(Y_5+Y_6)+Y_2Y_3(Y_7+Y_8)\right]}$$

The non-ideal transfer function for T_2

(Eq. 3.23)

$$T_2=\frac{V_2}{V_i}=\frac{\frac{\left[Y_5(Y_1+Y_3)(Y_4+Y_7+Y_8)\right]}{\omega_{t_1}}s+\left[Y_1Y_4Y_5+Y_1Y_5Y_8+Y_2Y_3Y_7-Y_1Y_6Y_7\right]}{\frac{(Y_1+Y_3)(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}\omega_{t_2}}s^2+\frac{Y_1(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}}s+\frac{Y_3(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_2}}s+\left[Y_1Y_4(Y_5+Y_6)+Y_2Y_3(Y_7+Y_8)\right]}$$

Where ω_{t1} and ω_{t2} are the *Gain Band-Width Product* (GBWP) of the two op amps used. Note that if ($\omega_t \to \infty$), assuming ideal op amps, the non-ideal transfer function equations simplify to the ideal equations from Table 3.1. These equations, along with switched-capacitor theory, will provide z-domain non-ideal transfer functions for the final circuit topology.

IV. SWITCHED CAPACITORS

Resistors are heavily used in filter design to set a multitude of operating characteristics for the device. Resistor values, in conjunction with capacitors, set ω_p and Q_p for the GIC filter. For a programmable GIC filter to be of practical use, it must be able to be fabricated using commercial IC processes and have predictable performance characteristics. Unfortunately, modern IC manufacturing techniques only produce resistors which have highly variable values. The tolerances can be as bad as 50-100% from specifications. [Ref. 8] Since center frequency of a filter is determined by the RC product as shown,

$$\omega_p = \frac{1}{RC} \qquad \text{(Eq. 4.1)}$$

a variation of 50% or more in a resistor value will cause unacceptably large variations in the filter's center frequency. The variations in the manufacturing processes which cause these wide ranges tend to show up between wafers and even in different areas of a given wafer, although they basically remain consistent across the small area of a given IC die. [Ref. 8] The consistency of variations within a given die is crucial for performance tolerances of the programmable GIC filter.

There is a way to get accurate resistors in ICs, but the drawback is a prohibitively expensive cost. Resistors can be measured after production and then laser trimmed to specifications. Unfortunately, this is time consuming and labor intensive. Chips of this nature are produced, but they are essentially custom and much more expensive than a batch process chip. Switched capacitors can alleviate this problem in IC filter design.

A. SWITCHED CAPACITOR BASICS

A switched capacitor is a circuit consisting of a capacitor and one or more switches. This circuit can be made to function as a resistor by alternately charging and discharging the capacitor from one node to another. The size of the equivalent resistance is determined by capacitor size and switching frequency. [Ref. 5] Figure 4.1 shows a basic switched capacitor circuit.

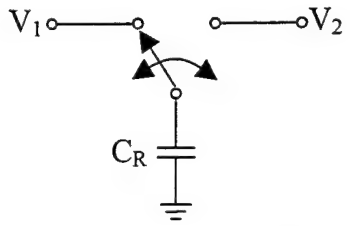

Figure 4.1: Simple Switched Capacitor Network. From Ref. [7]

The capacitor charges when the switch is connected to V_1 and discharges when connected to V_2. This moves a discrete amount of charge from node 1 V_1 to node V_2 for each switch cycle. The amount of charge moved over a time period is determined by switching frequency and the capacitor size. This circuit is very helpful in filter design because it allows the use of a ratio of capacitances to determine operating characteristics. Variations are uniform within each die, so all capacitances will vary by the same amount for a given chip. Thus, a filter can be designed with minimal variation from chip to chip. More detailed analysis of switched capacitor operation will show this advantage.

B. SWITCHED CAPACITOR DESIGN

1. Switched Capacitor Equivalent Resistance

Simple switched capacitor design and equations for equivalent resistance are developed in this section. Figure 4.2 shows actual implementation for a simple IC

switched capacitor.

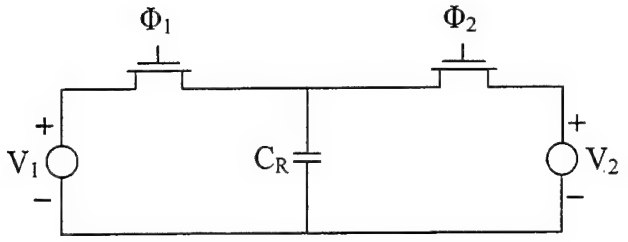

Figure 4.2: MOS Implementation of a Switched Capacitor. From Ref. [7]

Two CMOS transistors are used as passgates to perform the operation of the single switch from Figure 4.1. A two-phase non-overlapping clock controls the switching function of the gates of the CMOS transistors. The clock circuit design ensures only one switch is closed at any given time. During the switching, one transistor must be off before the other is turned on to prevent a short circuit and allow the circuit to function properly.

Operation is based upon stored charge Q on the capacitor. When Φ_1 is on (and Φ_2 off), capacitor C_R is connected to V_1. The capacitor charges to

$$Q_1 = C_R V_1 \qquad \text{(Eq. 4.2)}$$

When Φ_2 is turned on (and Φ_1 turned off) C_R charges to V_2. The charge flowing in the circuit is

$$Q_2 = C_R V_2 - C_R V_1 = C_R(V_2 - V_1) \qquad \text{(Eq. 4.3)}$$

This is the difference between the charge on C_R from V_2 and the previous charge on C_R from V_1. When the transistors are switched again, the charge becomes

$$Q_3 = C_R V_1 - C_R V_2 = C_R(V_1 - V_2) \qquad \text{(Eq. 4.4)}$$

This sequence of events continues while the circuit is switched. If the network is switched at

$$f_c = \frac{1}{T_c} \qquad \text{(Eq. 4.5)}$$

The average rate of charge transferred Q over period T_c acts as current flow. This is expressed as

$$I \cong \frac{\Delta Q}{T_c} = \Delta Q f_c = f_c C_R (V_1 - V_2) \qquad \text{(Eq. 4.6)}$$

Dividing the potential difference by I gives

$$R \cong \frac{V_1 - V_2}{I} = \frac{1}{f_c C_R} \qquad \text{(Eq. 4.7)}$$

The equivalent resistance of a switched capacitor network is given by Eq. 4.7. [Ref. 5]

2. Switched Capacitor Circuit Filters

Using switched capacitors to replace resistors gives a great advantage in IC fabrication. Comparing the RC product of a resistor R_1 and a capacitor C_2 gives an example. [Ref. 5] The time constant τ is given by

$$\tau = R_1 C_2 \qquad \text{(Eq. 4.8)}$$

This is the determining factor in the filter center frequency. τ must be kept as accurate as possible to keep variations low between chips. The accuracy dependence of τ upon R_1 and C_2 is given by

$$\frac{d\tau}{\tau} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} \qquad \text{(Eq. 4.9)}$$

The accuracy of τ is the sum of the absolute accuracy of R_1 and C_2. If we replace R_1 with a switched capacitor, τ becomes

$$\tau = \frac{1}{f_c}\frac{C}{C_R} = T_c\frac{C}{C_R} \qquad \text{(Eq. 4.10)}$$

The accuracy of τ now becomes

$$\frac{d\tau}{\tau} = \frac{dT_c}{T_c} + \frac{dC_2}{C_2} - \frac{dC_R}{C_R} \qquad \text{(Eq. 4.11)}$$

Assume that T_c is accurate (by using a high accuracy crystal controlled clock)

$$\frac{d\tau}{\tau} = \frac{dC_2}{C_2} - \frac{dC_R}{C_R} \qquad \text{(Eq. 4.12)}$$

The center frequency of a filter realized using switched capacitors is

$$\omega_p = \frac{C_R}{C} f_c \qquad \text{(Eq. 4.13)}$$

Where ω_p is the filter center frequency, which is equal to $1/\tau$. In IC technology, this ratio between two capacitors can be realized with a high degree of accuracy. Thus, IC implementation of filters using switched capacitor techniques allows accurate center frequencies. Typical tolerances for capacitor ratios can be better than 0.1%. [Ref. 5]

C. SAMPLED DATA SYSTEMS

The focus of this project is to develop an analog filter to replace digital filters in IC designs. To fully understand switched capacitor filter operation, the concept of sampled data signals must be introduced. Analog signals are continuous in both time and amplitude. Digital signals have discrete time components and quantized amplitude

components. Sampled data signals are discrete in time, but the amplitude is not quantized. Switched capacitor systems are sampled data systems. Clocking moves charge at discrete time intervals, but the signal is never converted to a quantized value. Thus the goal of eliminating quantization error, gaining a speed improvement, and a circuit complexity reduction (removing the need for A/D, D/A and microprocessor circuitry) of an analog system has been realized by using switched capacitors. The only change in design procedures required is using a *z*-transform, which moves the design process out of the *s*-domain to the *z*-domain.

There have been four transformation methods used to analyze and design switched capacitor networks. These are the *Backward Difference*, the *Forward Difference*, the *Bilinear*, and the *Lossless Discrete Integrator*. [Ref. 1] Previous work has shown the bilinear transform to be appropriate for this design. [Ref. 7] The bilinear transformation is given by

$$\frac{1}{s} = \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}} \qquad \text{(Eq. 4.14)}$$

or

$$s = \frac{2}{T}\frac{z-1}{z+1} \qquad \text{(Eq. 4.15)}$$

The main side effect of the bilinear transformation that must be taken into account is frequency warping. This warping results from a nonlinear relationship between the analog frequency ω_s, where $s = j\omega_s$, and the sampled data domain frequency ω, where $z = e^{j\omega\gamma}$. [Ref. 1] The warping can be shown by placing $s = j\omega_s$ and $z = e^{j\omega\gamma}$ into Eq. 4.15 and dividing numerator and denominator by $2e^{j\omega T/2}$

$$\frac{\omega_s T}{2} = \tan\frac{\omega T}{2} \qquad \text{(Eq. 4.16)}$$

Solving for ω,

$$\omega = \frac{2}{T}\tan^{-1}\left[\frac{\omega_s T}{2}\right] \qquad \text{(Eq. 4.17)}$$

The frequency change from sampling is given by Eq. 4.17. [Ref. 1] There are two ways to compensate for this warping effect. One is to pre-warp the desired filter frequencies during the design process. The other minimizes the warping by using a clock signal at least ten times faster than the analog signal of interest. Warping effects can be ignored if this separation is maintained.

D. FLOATING BILINEAR SWITCHED CAPACITOR RESISTORS

The switched capacitor topology used in this filter is the *Floating Bilinear Resistor (FBR)*. Configuration for a FBR is shown in Figure 4.3, with Φ_e representing even clock pulses and Φ_o representing odd clock pulses.

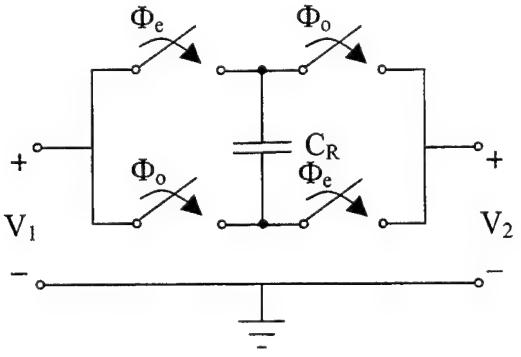

Figure 4.3: Floating Bilinear Resistor. After Ref. [1]

Using previous research, the equivalent admittance for a FBR is shown, [Ref. 6] with $z = e^{s\tau}$

$$y_R = C\left(1 + z^{\frac{-1}{2}}\right) \qquad \text{(Eq. 4.18)}$$

or with $\hat{z} = e^{\frac{s\tau}{2}}$

$$y_R = C\left(1 + \hat{z}^{-1}\right) \qquad \text{(Eq. 4.19)}$$

Eqs. 4.18 and 4.19 give equivalent admittance for a FBR in terms of z. To develop equations not dependent on z, another equation for the admittance of a FBR is required. Taking the Laplace domain admittance for a resistor and using the bilinear transformation (Eq. 4.15) to change it to the z-domain generates this equation. Table 4.1 gives the Laplace domain admittances of circuit components and their equivalent admittance transformed to the z-domain by the bilinear transformation.

	Circuit Element		
	Capacitor	**Resistor**	**Inductor**
Laplace Domain Admittance	sC	G	1/sL
Z-Domain Admittance after Bilinear Transform	$C\left(1 - z^{-1}\right)$	$\frac{G\tau}{2}\left(1 + z^{-1}\right)$	$\frac{\tau^2}{4L}\frac{\left(1 + z^{-1}\right)^2}{1 - z^{-1}}$

Table 4.1: Equivalent Admittances. After Ref. [1]

Setting admittance of Eq. 4.18 equal to Table 4.1, for the half clock cycle

$$C\left(1 + z^{-1}\right) = \frac{G\tau\left(1 + z^{-1}\right)}{2} \qquad \text{(Eq. 4.20)}$$

Solving Eq. 4.19 for G

$$G = \frac{2C}{\tau} \qquad \text{(Eq. 4.21)}$$

Using Eq. 4.18, the equivalent admittance for a full clock cycle is

$$G = \frac{4C}{\tau} \qquad \text{(Eq. 4.22)}$$

These equations give the equivalent resistance of the floating bilinear resistor, which will be used in the design of the GIC filter.

E. TWO PHASE NON-OVERLAPPING CLOCK

In order for this switched capacitor network to function properly, a specialized clock circuit must be developed. This clock circuit provides a method to switch the transistors. To prevent a short circuit path from one node to another, thus bypassing the capacitor, the clock signals must ensure the opposite transistor is being turned off before the other transistor turns on. Figure 4.4 shows the output required of the non-overlapping clock circuit.

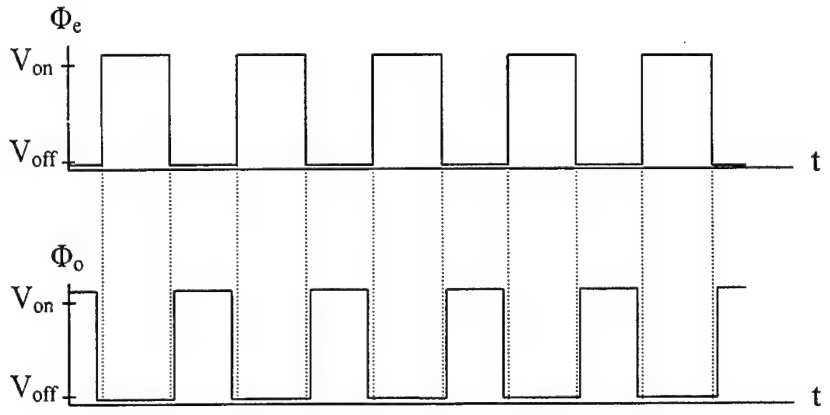

Figure 4.5: Two Phase Non-Overlapping Clock Output. From Ref. [7]

The circuit that can deliver this clock performance will be developed in Chapter VI.

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V. VLSI DESIGN PRINCIPLES

Complementary Metal Oxide Silicon (CMOS) technology is used in the implementation of the Digitally Programmable GIC Filter. J. Lilienfeld discussed the basic principles used by the *MOS Field-effect Transistor* (MOSFET) as early as 1925. Early experiments with FETs encountered material problems and eventually led to the invention of the bipolar transistor. The success of this device pushed aside the MOSFET until the 1960s. Material and quality-control problems still hampered the MOSFET until 1967 when Fairchild Semiconductor had a patent granted for CMOS concepts that covered the basic building blocks of the *Inverter*, *NAND Gate*, and *NOR Gate*. Since that time, CMOS technology has grown to become the dominant form of VLSI design. [Ref. 9]

A. SILICON SEMICONDUCTOR TECHNOLOGY BASICS

Pure silicon is a semiconductor, which means its resistance to electrical current flow is between that of an insulator and a conductor. By placing small amounts of impurities within the silicon lattice, the resistivity can be greatly reduced. Impurities that place extra electrons in the material are called *Donors*, while those that create electron vacancies in the silicon crystal are called *Acceptors*. Acceptors bind electrons to the impurity atoms and thus produce an excess of holes in the material. When donors dominate, the material is *n-type*. A dominance of acceptors produces *p-type* material. Placing n-type and p-type materials together creates a junction, as in the case of a diode construction. [Ref. 9] Creating p-n-p or n-p-n structures is used to produce transistors. VLSI technology is the process of mass-producing these structures on a microscopic scale and connecting them as circuits.

1. Silicon Wafers

The basic foundation for semiconductor structures is the silicon wafer. This is a disk of silicon ranging from 75 mm to 300 mm in diameter and is less than 1 mm thick (usually about 600 μm). To produce a wafer, a silicon ingot must be grown first. Figure 5.1 shows the basic process. A seed crystal having the desired crystal orientation

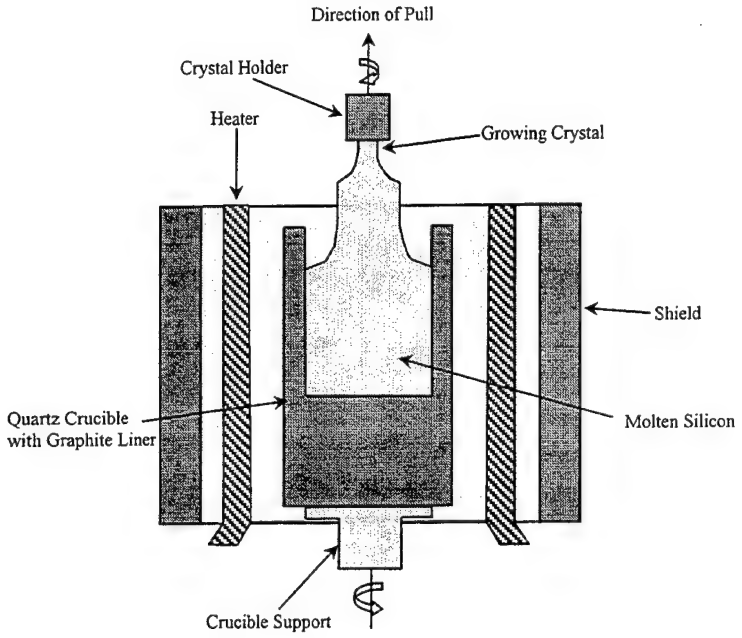

Figure 5.1: Silicon Ingot Growth Process. After Ref. [9]

is placed in a holder. Pure silicon is placed in the crucible and melted at ≈1425°C. Additional impurities are added to make the bulk crystal slightly n-type or p-type, if desired. The seed is then dipped into the melt and slowly withdrawn while being rotated. The molten silicon freezes to the seed crystal with the same crystal orientation. The seed is withdrawn and rotated at a rate to produce the desired diameter for the cylindrical ingot. This is then sliced into wafers using a diamond bladed saw. The wafer is then polished to a mirror finish. [Ref. 9]

2. Oxidation

Silicon Dioxide (SiO_2) is grown from the wafer or deposited on the wafer to produce many integrated circuit structures. SiO_2 is an insulator which prevents electrical current flow. The two main processes for field oxide growth are *Wet Oxidation* and *Dry Oxidation*. Wet oxidation creates an atmosphere above the wafer that has water vapor. The temperatures used are 900°C-1200°C and it is a rapid process. Dry oxidation uses a pure oxygen atmosphere and requires temperature in the 1200°C region to get an acceptable growth rate. These processes consume silicon from the wafer. The oxide grows down into the silicon wafer, but since the volume of the oxide is about twice as much as silicon, there will be about the same thickness of oxide above the initial non-oxidized silicon surface as below. [Ref. 9]

3. Creation of Impurities

Semiconductor structures are created by specific placement of differing levels of impurities near each other. The placement of impurities is achieved through several different processes. Some of these are *Epitaxy*, *Deposition*, *Diffusion*, and *Ion-Implantation*. Epitaxy is the process of growing a single-crystal film on the silicon surface by elevating the temperature and introducing the new material. Deposition introduces an evaporated dopant atmosphere and elevates the temperature to allow impurity atoms to permeate into the bulk silicon. Ion-Implantation focuses a high-powered beam of dopant material onto the region desired, which forces the impurities into the bulk silicon. Diffusion is the process of impurities spreading from regions of high concentration to lower concentration at elevated temperatures.

Amounts and location of impurities must be controlled to achieve the desired structures. The time of exposure and either energy of the beam for ion-implantation or temperature for diffusion determine the density of dopants. Masking areas to prevent the beam from penetrating the silicon or not allowing a dopant to contact the silicon surface controls the location of impurities. Places that have no mask allow the desired impurities in. Once it is no longer needed, the mask is removed and the process begins again for the next structure in the device. *Photoresist*, *Polycrystalline Silicon* (polysilicon or poly), and SiO_2 are commonly used for masking.

The process for creating these masks is called *Photolithography*. Figure 5.2 shows the basic photolithography process. Step 5.2.a is the bulk silicon wafer. Step

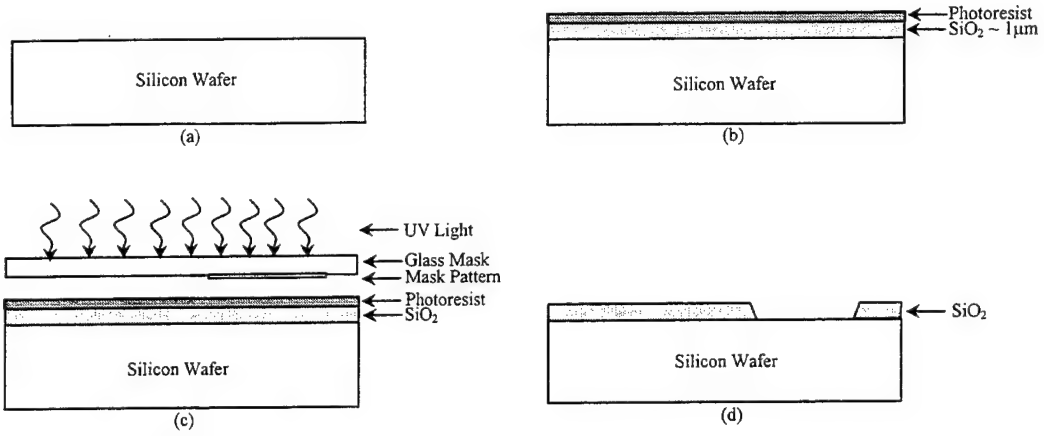

Figure 5.2: Photolithography Steps. After Ref. [9]

5.2.b grows a SiO_2 layer and then deposits a layer of photoresist solution. Step 5.2.c places a mask with the desired pattern over the wafer and exposes the photoresist to UV light, which hardens the resist (in a negative resist process, in a positive resist process the light weakens the resist). Step 5.2.d uses a solvent to remove the unexposed resist. An acid is applied which etches the SiO_2 not protected by resist. After the oxide is etched

away from the pattern area, the resist is removed with another solvent, usually an organic solvent such as acetone. This region can now be doped with the desired impurities. Once this step is complete, the process will be repeated with a different mask to make the next structure. [Ref. 9] Repeated applications will eventually grow a multi-layer device of the desired type.

B. CMOS N-WELL INVERTER CONSTRUCTION

The technology used to create this filter is an *n-well* process. Using an n-well

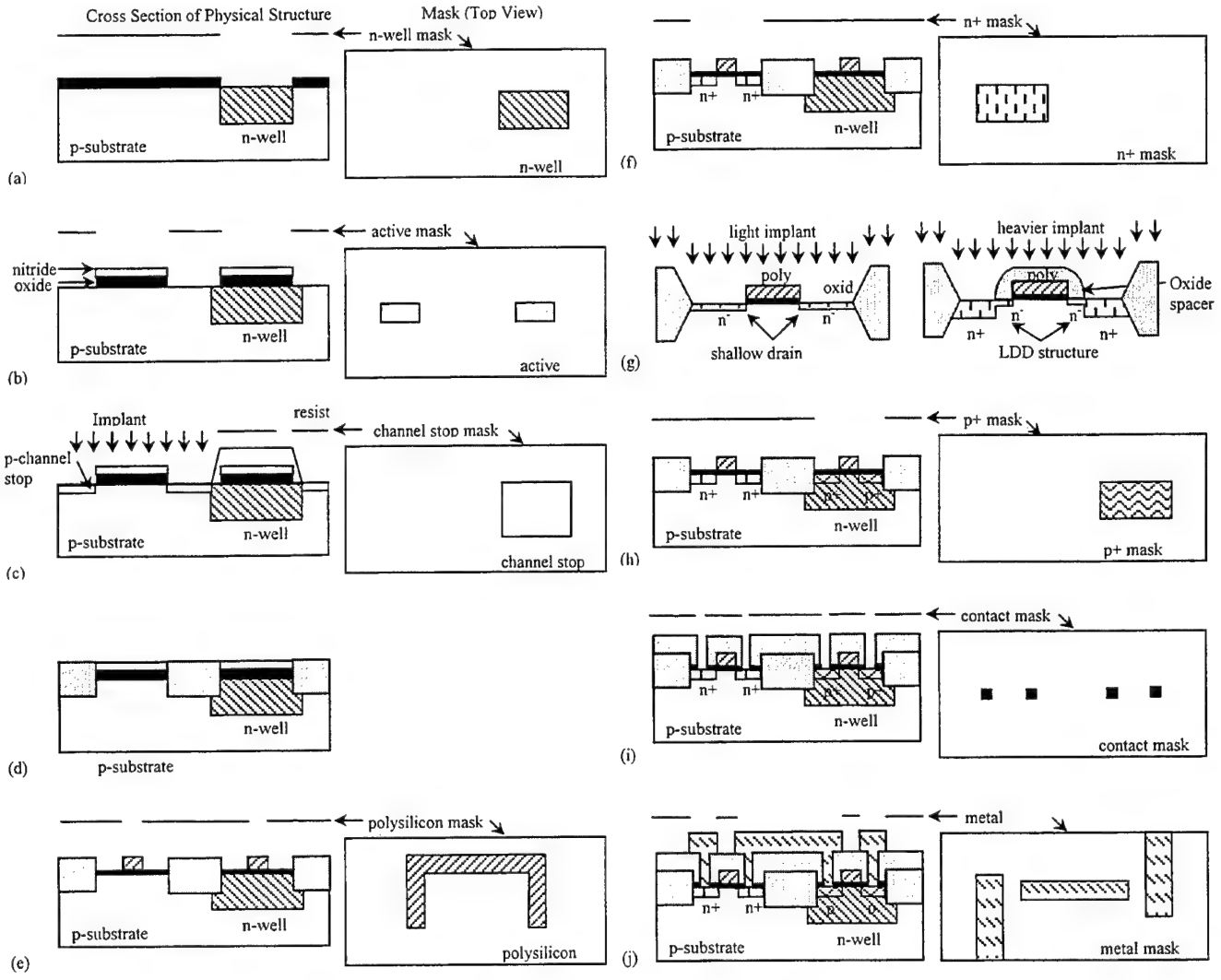

Figure 5.3: N-Well CMOS Process. After Ref. [9]

process allows the creation of p-type as well as n-type transistors. Figure 5.3 and the following description illustrate the creation of a basic inverter. Many growth, exposure and etching steps are lumped together into these larger step descriptions. Step 5.3.a takes a lightly p-type doped silicon wafer and makes an n-well. This area is doped with donors to make the region n-type. Step 5.3.b creates the *Active* regions. These are the locations where the gate regions and source and drain contacts of the transistor will be located. A *Thin Oxide* (thinox) of higher quality than the field oxide is placed in these locations. This oxide is then covered by SiN, which is used as a mask for the following two steps. Step 5.3.c creates a *Channel Stop*. The areas where there are no active regions or n-wells are now doped to a higher level p-type material to prevent leakage between transistors. Step 5.3.d grows a thick field oxide in all the regions without the SiN masking layer. The figure also shows the area has been *Planarized* to remove irregular heights on the oxide. Step 5.3.e removes the SiN and places the polysilicon gates on the thinox. Step 5.3.f heavily dopes the active region n-type, with the polysilicon acting as a self-aligning mask for the gate region of the *NFET* (n-type MOSFET). This creates the n-p-n structure. Step 5.3.g shows in detail the gate alignment and how channel edges are made thin with the first implant. Oxide is then grown over the polysilicon gate contact and the second implant supplies a greater level of doping. This helps to prevent diffusion of donors under the gate region, and keeps the gate region thin. This allows greater reliability for the device and gives greater control of the transistor by the gate voltage. Step 5.3.h repeats the process for the *PFET* (p-type MOSFET) to create the p-n-p structure. Step 5.3.i grows an isolating layer of field oxide and then etches the contacts to source and

drain regions of the transistor. Step 5.3.j places the metal contacts and circuit connections onto the device. [Ref. 9]

Figure 5.4 gives different representations and views for an n-well inverter. 5.4.a shows the schematic-view of the inverter, while 5.4.b shows top-view. Figure 5.4.c is an

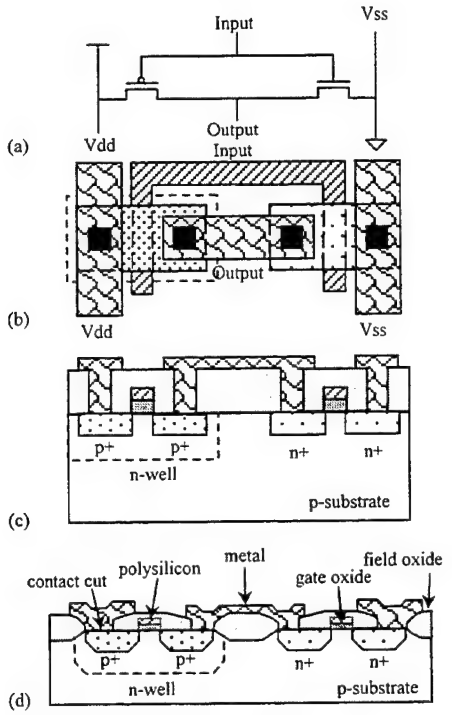

Figure 5.4: CMOS Inverter Cross Section. After Ref. [9]

idealized side-view, while 5.4.d is more realistic by showing the elevation variations that will be observed after the completion of fabrication. Figure 5.5 shows the cross section

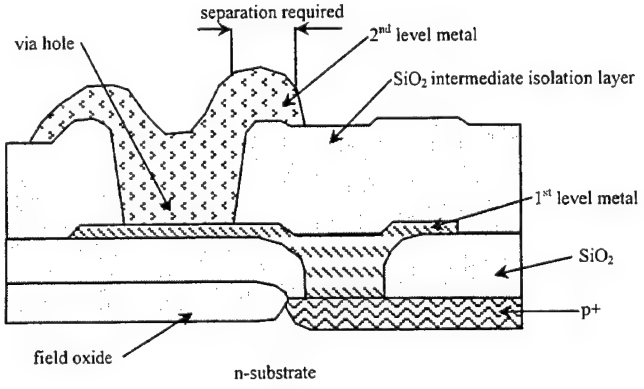

Figure 5.5: Two-Layer Metal Cross Section. After Ref. [9]

for two-layer metal lines used in our n-well process. Multiple layers of metal greatly reduce layout area and simplify the routing for circuit connection of the devices. The connections from first level metal to active regions or polysilicon are called *Contacts*. The connections between metal levels are called *Vias*.

The other structure used by the GIC filter besides the transistor is the capacitor. All the electrically isolated layers in the CMOS process have an associated capacitance based upon area of overlap. In most circuits, this is not desirable because the increase in parasitic capacitance causes a reduction in circuit speed. Therefore, most designs do not have large areas of overlap. We can take the two layers with the largest capacitance for unit area and overlap them. The desired capacitor can be achieved by making an appropriate size of overlap. In this n-well process, the polysilicon and n+-active regions have the largest capacitance and are used to make the capacitors.

C. DESIGN RULES

Design rules are layout size and distance spacing requirements a process requires to ensure areas can be patterned properly. They are usually a compromise to achieve a balance of yield and performance at the feature size technology being used. These design rules allow for standard variation in the processing of each wafer and ensure feature size variation and misalignments are tolerable and do not create shorts or opens in the circuit. This project uses a CMOS process that allows for gate lengths of 2 μm. Most design rules are *Scalable*, in that they allow the design to be shrunk as gate length and feature size improvements are made. Design rule distances are given in terms of λ, with the size of λ being adjusted to the technology used to fabricate the design. In this project λ is

1 μm. Figure 5.6 gives the design rules for this project. Layout of devices given in Chapter VII conforms to these design rules.

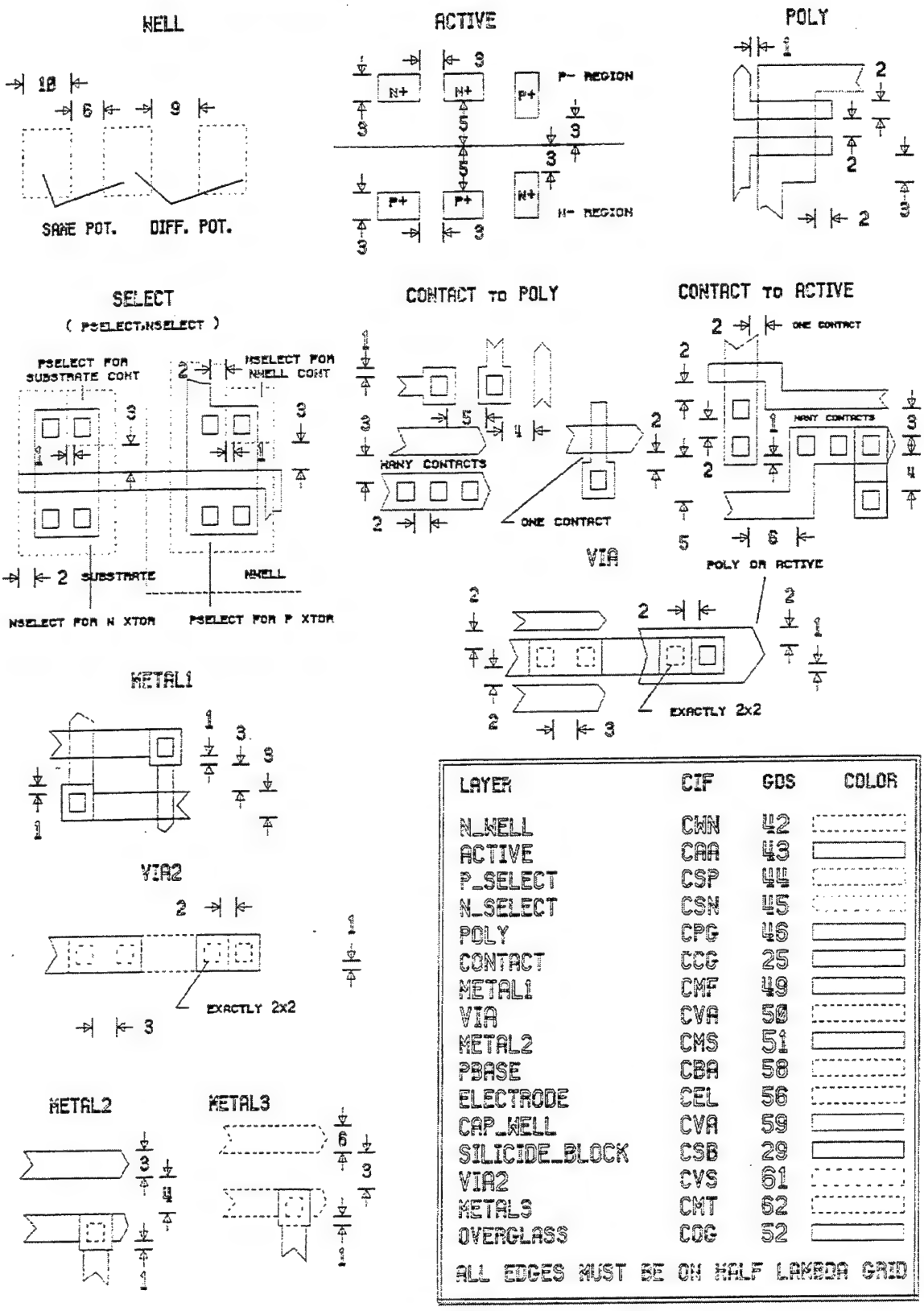

Figure 5.5: CMOS Design Rules. From Ref. [10]

VI. DIGITALLY PROGRAMMABLE GIC FILTER

The goal of this research is to produce a digitally programmable filter. This allows the fabrication process to produce the same chip at high volume, thus reducing costs, while still allowing the end user maximum flexibility in the chip application. This chapter will develop the selection logic to change topology, center frequency and quality factor with a simple 8-bit binary input. Selectable frequencies will be developed for a 10 MHz input clock and a basic capacitor size of 2 pF for the bilinear resistors. If desired, the user could input a lower clock frequency to change the frequency selection range as well.

A. TOPOLOGY SELECTION

From Table 3.1, appropriate elements for the GIC sections can be chosen. Four combinations of eight switch signals are needed to change the topological configuration of the filter circuit. Table 6.1 gives the truth table for required logic using bits S0 and S1 of the binary selection word.

Input		**Topology Controls**								**Topology**
S0	S1	TC0	TC1	TC2	TC3	TC4	TC5	TC6	TC7	
0	0	0	1	1	0	1	0	1	0	Notch
0	1	1	0	1	0	1	0	0	1	High Pass
1	0	1	0	1	0	0	1	0	1	Band Pass
1	1	0	1	0	1	0	0	0	1	Low Pass

Table 6.1: Topology Selection Truth Table. After Ref. [7]

The circuit to produce this truth table is shown in Figure 6.1. The topology logic block uses inverters and nand gates to produce digital control signals. These logic signals are asynchronous and control single input passgate switches. By turning various switches

on and off, all four topologies can be realized utilizing only four floating bilinear resistor blocks (G), two variable capacitor blocks (C), one variable floating bilinear resistor

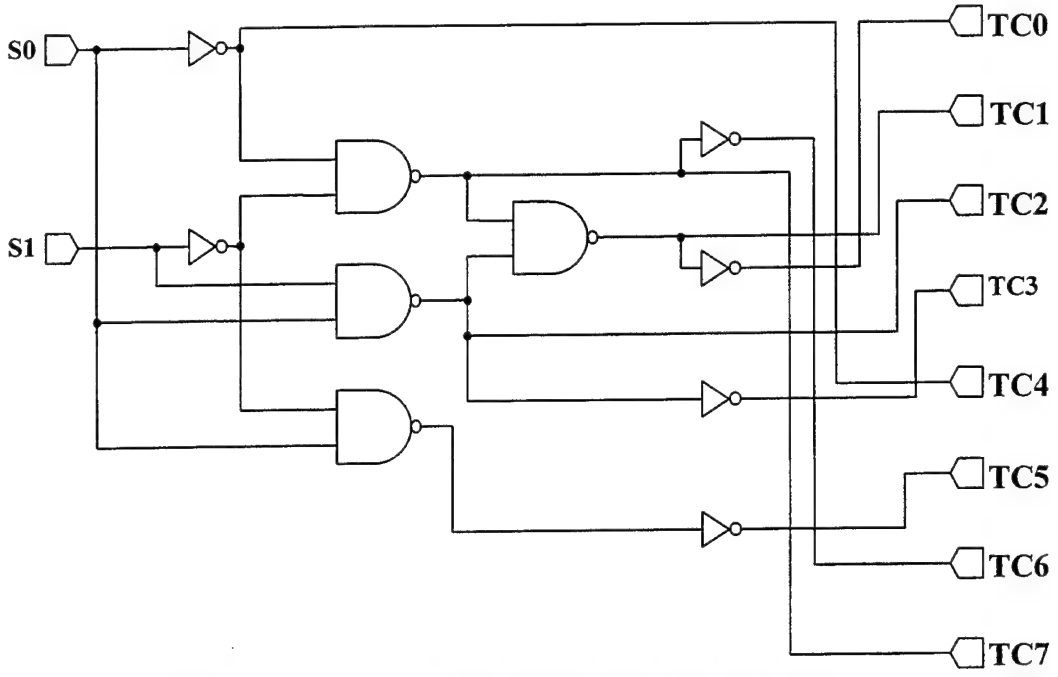

Figure 6.1: Topology Selection Circuit. After Ref. [7]

block (G_Q) and two op-amps. The filter with topology switches is shown in Figure 6.2.

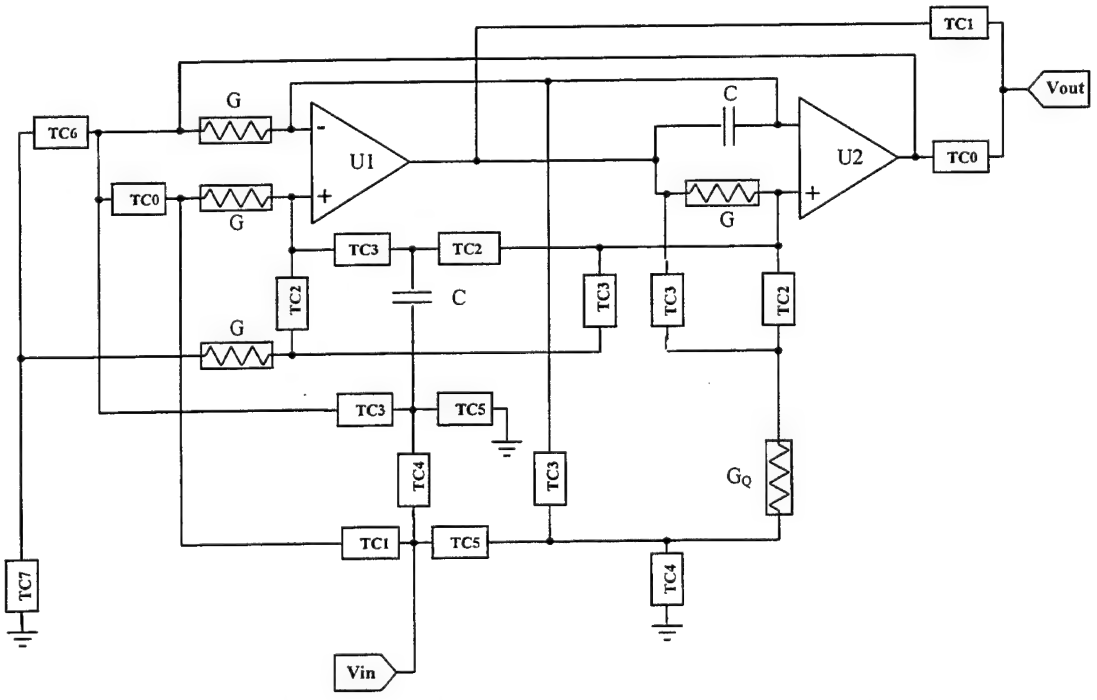

Figure 6.2: GIC Filter with Topology Switches. After Ref. [6]

B. CENTER FREQUENCY SELECTION

Frequency selection is accomplished by changing the size of capacitor elements from Table 3.1. Table 6.2 gives the truth table for required logic using bits S2, S3 and S4 of the binary selection word. Control signals are sent to binary-weighted capacitor banks. The maximum ω_c for a 10 MHz clock is limited to 1 MHz to minimize warping. Basic capacitor size was chosen using Eq. 4.13 to give a center frequency of 1 MHz. The binary-weighted values were then applied to Eq. 4.13 to produce the rest of the selectable center frequencies. Using a different clock frequency allows a linear shift in the selectable frequency range. Figure 6.3 shows frequency selection circuit.

Input			Frequency Controls			Capacitance	Frequency
S2	S3	S4	FC0	FC1	FC2		
0	0	0	0	0	0	13 pF	994.1 KHz
0	0	1	1	0	0	26 pF	497.1 KHz
0	1	0	0	1	0	39 pF	331.3 KHz
0	1	1	1	1	0	52 pF	248.5 KHz
1	0	0	0	0	1	65 pF	198.8 KHz
1	0	1	1	0	1	78 pF	165.7 KHz
1	1	0	0	1	1	91 pF	142.0 KHz
1	1	1	1	1	1	104 pF	124.0 KHz

Table 6.2: Frequency Selection Truth Table. After Ref. [7]

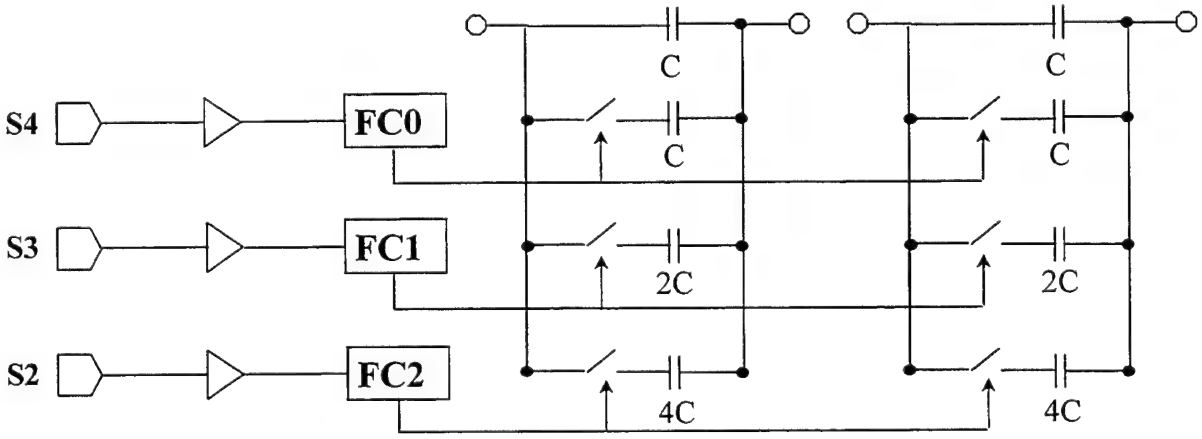

Figure 6.3: Frequency Selection Circuit.

C. QUALITY FACTOR SELECTION

A variable FBR controls the quality factor. This is accomplished with a 2 pF capacitor and two 1 pF capacitors utilizing different series connection topologies. Placing the capacitors in series, which changes the value of G_Q, by reducing the equivalent capacitance. Table 6.3 gives the truth table for the quality factor selection logic using bits S5, S6 and S7 of the binary selection word.

Input			Quality Factor Controls							Quality Factor
S5	S6	S7	QC0	QC1	QC2	QC3	QC4	QC5	QC6	
0	0	0	0	1	1	0	1	0	0	5
0	0	1	0	1	1	1	1	0	0	4
0	1	0	0	1	0	0	0	0	1	1
0	1	1	0	1	1	1	0	0	1	0.8
1	0	0	1	0	0	0	1	1	0	2
1	0	1	1	0	0	1	1	1	0	Not Used
1	1	0	1	0	0	0	0	0	1	Not Used
1	1	1	1	0	0	1	0	0	1	3

Table 6.3: Quality Factor Selection Truth Table. After Ref. [7]

Figure 6.4 shows the quality factor selection circuit. Φ_o and Φ_e represent the odd and even signals from the non-overlapping clock.

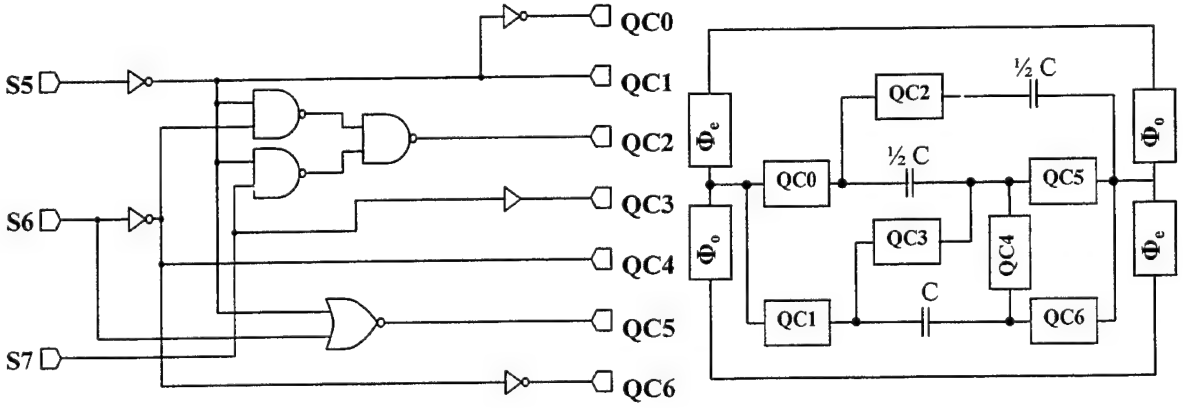

Figure 6.4: Quality Factor Selection Circuit. After Ref. [7]

D. TWO PHASE NON-OVERLAPPING CLOCK

To implement the FBR blocks, a two phase non-overlapping clock is required. The desired performance required, shown in Figure 4.5, can be achieved with a simple circuit utilizing inverters and two nand gates. This configuration allows one clock signal to go low before the other goes high, thus preventing a short circuit condition in the filter. Figure 6.5 illustrates the circuit schematic.

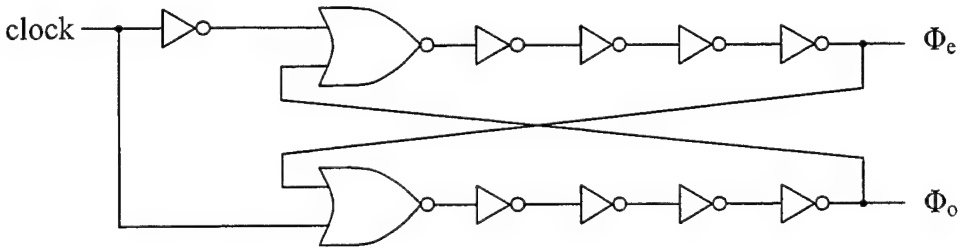

Figure 6.5: Two Phase Non-Overlapping Clock Circuit. After Ref. [7]

The following chapter will demonstrate the VLSI layout of the filter and PSPICE simulations will be carried out.

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VII. VLSI GIC FILTER LAYOUT AND SIMULATION

After completing a symbolic design for the filter, the circuit must be laid out using VLSI software to create masks for the fabrication process. This project used LASI 6.0, a free for non-profit use program, written by D. Boyce. The logic level design from Chapter VI is converted to transistor level schematics for each block, then these blocks add together forming an overall transistor level schematic. Once schematics are done, each block is mapped out according to the design rules. When all blocks are complete, a node check is run to ensure that the nodes in the physical layout match the nodes in the schematic. Following the node check, a design rule check is run to ensure that none of the design rules are violated. Lower level blocks are then placed into a higher level block and interconnects are made. The process of building increasingly higher level blocks, verifying node and design rule compliance at each step, is continued until the chip is completed. Once complete, a file containing layer specifications is created and sent to the fabricator who will create physical masks from the file and fabricate the chip. MOSIS is used for the fabrication of this chip.

Simulation of the circuit was conducted with MicroSim PSPICE version 8.0. Transistor models used in the simulation are from MOSIS measurements for this n-well process.

A. FUNCTIONAL BLOCKS

The first step for chip creation is determining functional blocks for the overall design and determining inputs, outputs, and interconnects between these blocks. These functional blocks were defined in Chapter VI during the symbolic design of the filter.

Figure 7.1 shows functional blocks and highlights inputs, outputs and interconnects between blocks.

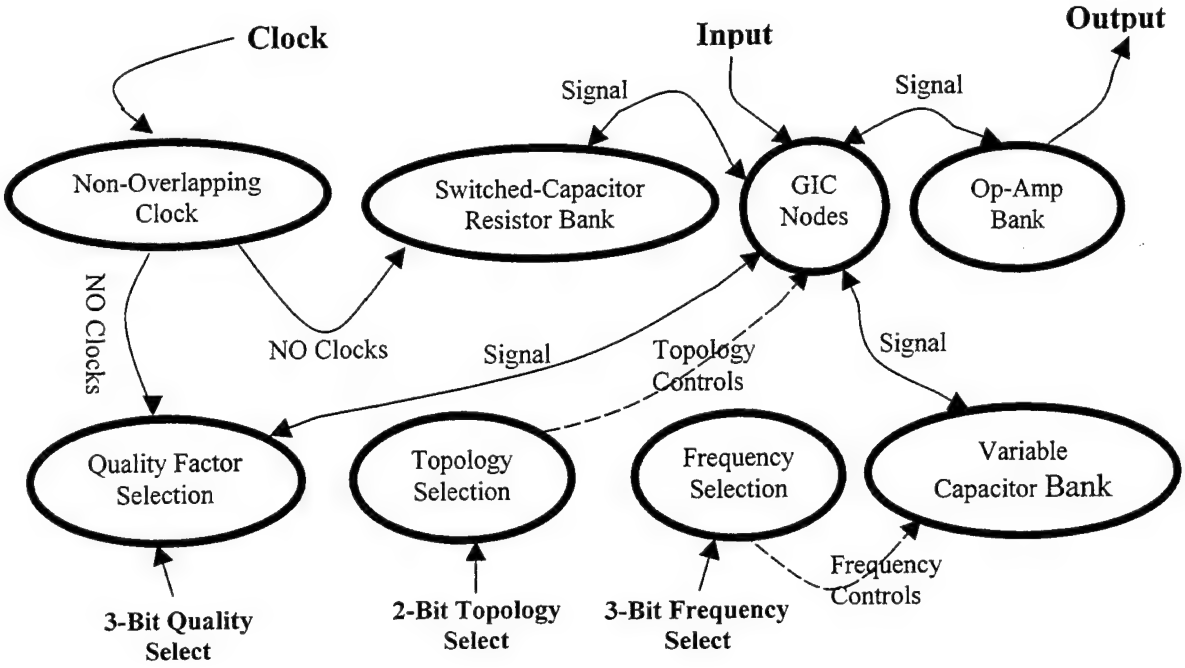

Figure 7.1: GIC Filter Functional Blocks.

B. BASIC COMPONENTS

Transistors and capacitors are the two most basic components in this design. Chapter V described how both devices are created during the VLSI fabrication process. Tailoring the size of these two basic components and connecting them in various ways creates the larger devices in this design. The following discusses an inverter using two transistors. Additionally, three transistor models are shown in Appendix A.

This design uses three different size inverters. The logic sections and single input switches use minimum size inverter. The non-overlapping clock uses the other two sizes. Figure 7.2 shows an output inverter used in the non-overlapping clock circuit in detail to highlight different areas and explain the mask levels displayed by LASI. The output

inverter shown in Figure 7.2 consists of a 2 μm by 12 μm NFET and a 2 μm by 40 μm PFET. NFETs in this process are about 3.3 times faster than PFETs. By designing gate

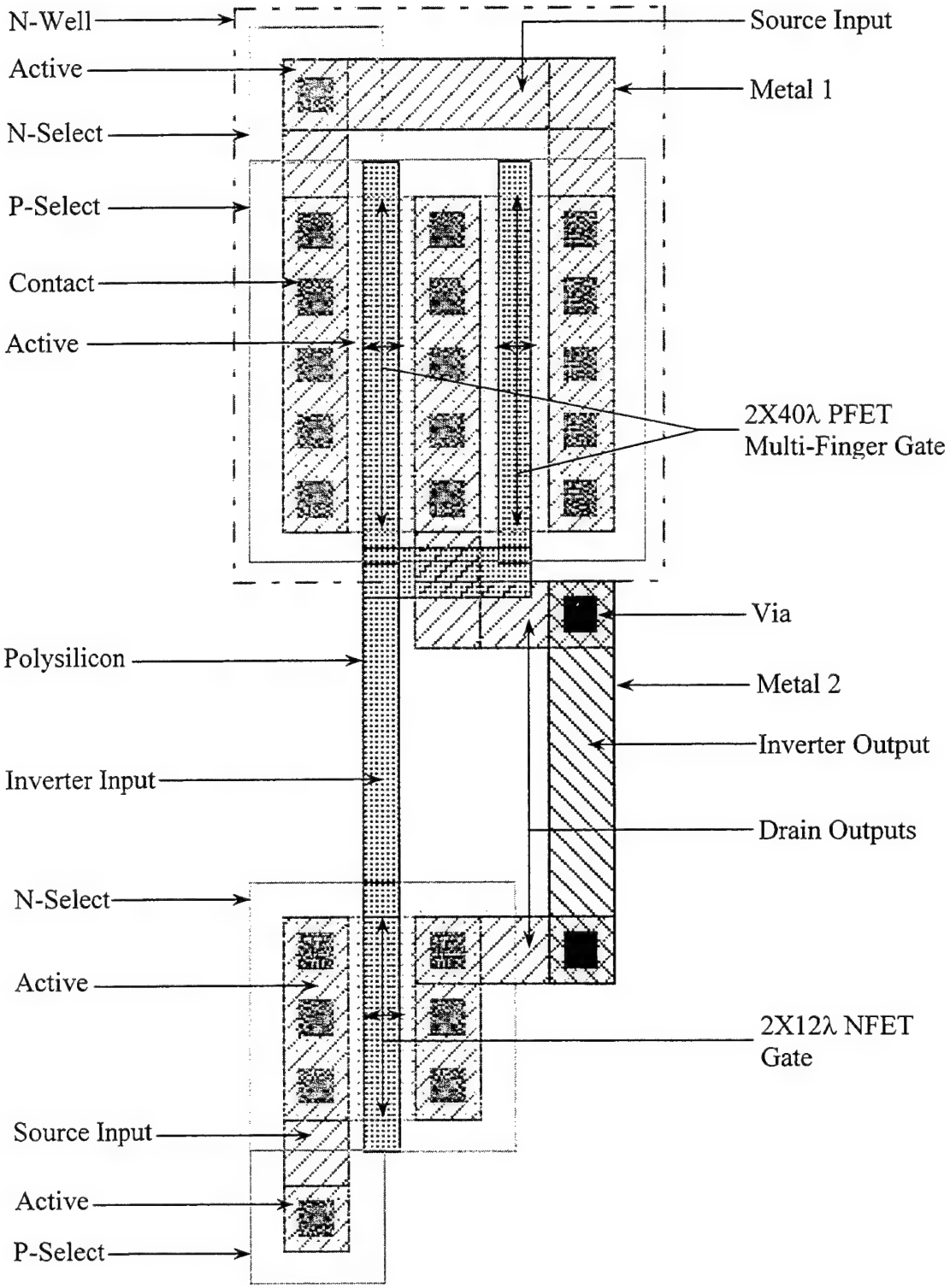

Figure 7.2: Non-Overlapping Clock Output Inverter.

widths for PFETs larger, transistor gain is matched and corresponding switching response becomes symmetrical. The square *Select* areas of opposite polarity on each transistor are substrate and well contacts. These prevent *Latch-Up* (turning on a parasitic *Bipolar Junction Transistor* (BJT)), which can burnout the transistor, by shorting source contacts to substrate or well potential. This prevents parasitic BJTs from turning on and destroying the MOSFET. Layouts for following structures are found in Appendix A.

Buffers are composed of two minimum sized inverters in series. NAND gates are composed of two NFETs in series and two PFETs in parallel as shown in Figure 7.3. Layout area can be saved by using the same active areas for same type transistor pairs.

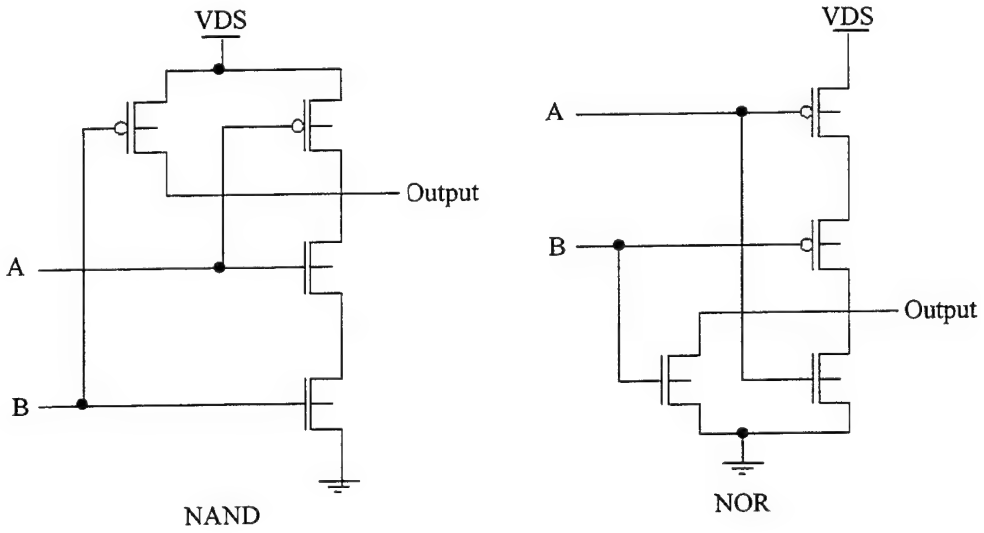

Figure 7.3: NAND and NOR Gates.

NOR gates are composed of two NFETs in parallel and two PFETs in series, also shown in Figure 7.3. The use of the same active areas is again used to save layout area.

Capacitors consist of overlapping sections of polysilicon and n+-active. The overlap capacitance of these two layers is 1131 aF/μm^2, while the fringing capacitance is

187 aF/μm. A 42 μm by 42 μm overlap produces 2.03 pF of capacitance. Additionally, the filter uses 1 pF and 13 pF capacitors.

This filter uses two types of passgates. The basic passgate is composed of one NFET and one PFET. The gates take opposite switch signals to turn each transistor on. The input signal is tied to the source of both transistors and the output is taken from the drain of both transistors. Two transistors are used such that the signal level will be the same whether it is high or low. A single NFET transistor switch would perform strongly with a low signal, but weakly with a high signal. The opposite is true for a single transistor PFET switch. Two-input passgates are used in the FBRs and take an input from the even phase of the clock and the other input from the odd phase of the clock. Logic sections use one-input passgates, which are composed of an inverter and a two-input passgate. The passgate uses the switch signal for one gate and the inverted signal for the other gate.

Table 7.1 illustrates *Noise Margins* (NML – Low; NMH – High), *Rise Times* (T_R), *Fall Times* (T_F), *Time Delays* (T_{PLH} – Low to High; T_{PHL} – High to Low), and *Peak Powers* (P_M) for the basic components.

Component	NML	NMH	T_R	T_F	T_{PLH}	T_{PHL}	P_M
INVMIN	1.47 V	1.74 V	0.80 ns	0.74 ns	0.47 ns	0.48 ns	625 μW
INVCLKM	1.45 V	1.73 V	0.56 ns	0.56 ns	0.32 ns	0.37 ns	1245 μW
INVCLKO	1.42 V	1.66 V	0.54 ns	0.51 ns	0.31 ns	0.26 ns	2450 μW
$NAND_{\Delta 1\text{-Input}}$	0.88 V	2.15 V	0.86 ns	0.73 ns	0.49 ns	0.39 ns	850 μW
$NAND_{\Delta 2\text{-Inputs}}$	1.99 V	1.22 V	-	-	-	-	-
$NOR_{\Delta 1\text{-Input}}$	1.70 V	2.23 V	0.99 ns	1.17 ns	0.60 ns	0.74 ns	710 μW
$NOR_{\Delta 2\text{-Inputs}}$	0.98 V	2.16 V	-	-	-	-	-

Table 7.1: Basic Component Simulation Results.

C. TWO PHASE NON-OVERLAPPING CLOCK

The two phase non-overlapping clock was created using the basic components according to design from Chapter VI. Figure 7.4 shows a transient analysis of the clock's performance. Figure 7.5 is a closer view of the switching behavior. The circuit was

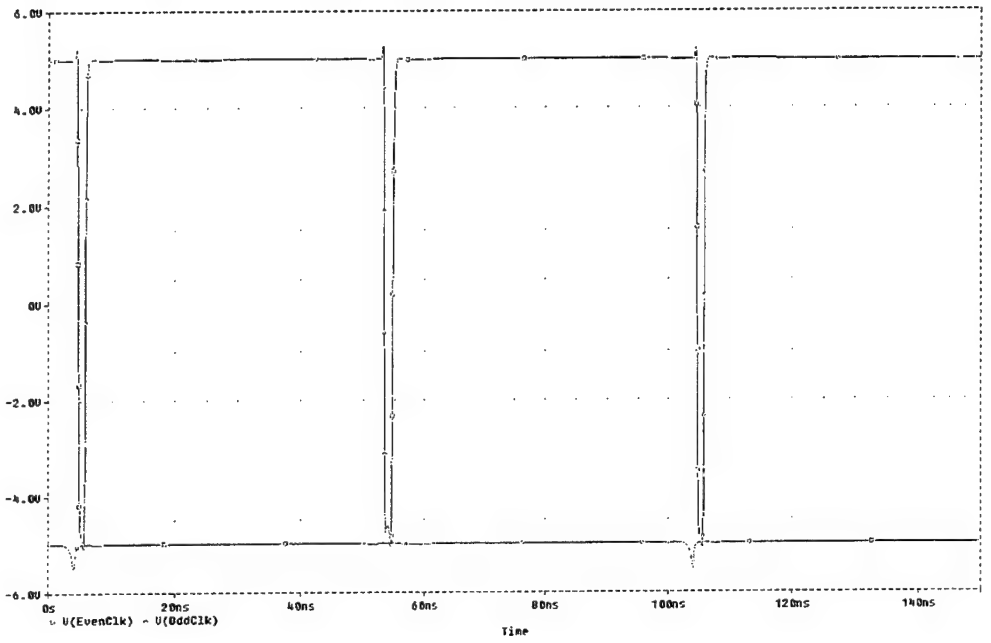

Figure 7.4: Two Phase Non-Overlapping Clock.

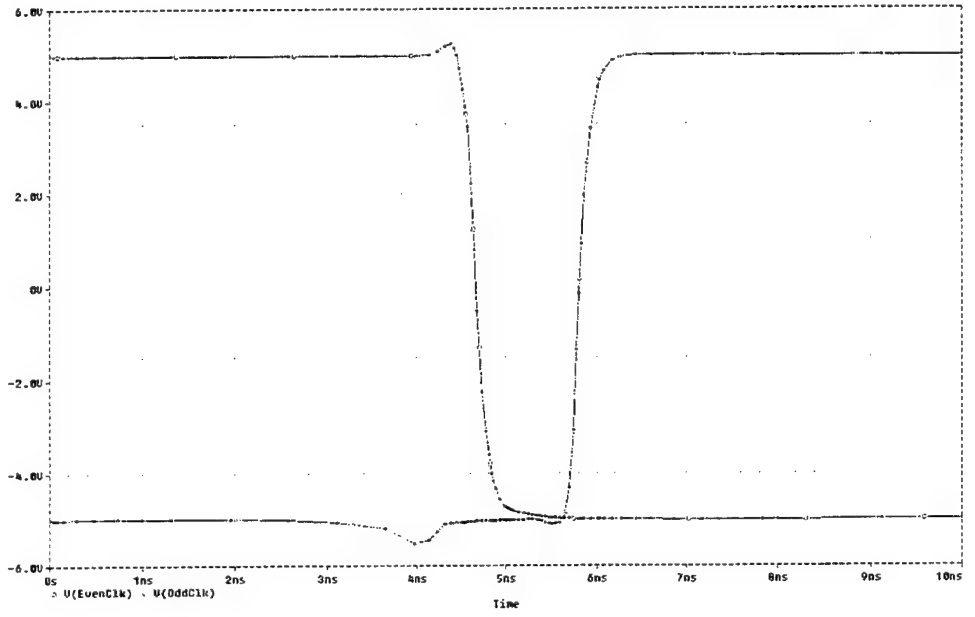

Figure 7.5: Two Phase Non-Overlapping Clock Zoom.

simulated with a 10 MHz clock input. The clock maintains its non-overlapping character up to approximately 125 MHz. Although this frequency would be desirable, the switching time becomes too large of a portion of the waveform period to maintain proper operation for the circuit. 10 MHz provides adequate performance and allows filter operation at signal frequencies up to 1 MHz, a limitation also imposed by the op amps.

D. FLOATING BILINEAR RESISTORS

Converting Eq. 4.22 from admittance to resistance and τ to f_c yields

$$R = \frac{1}{4C_R f_C} \qquad \text{(Eq. 7.1)}$$

Setting C_R = 2.03 pF and fc = 10 MHz makes R = 12315 Ω. This is the size for

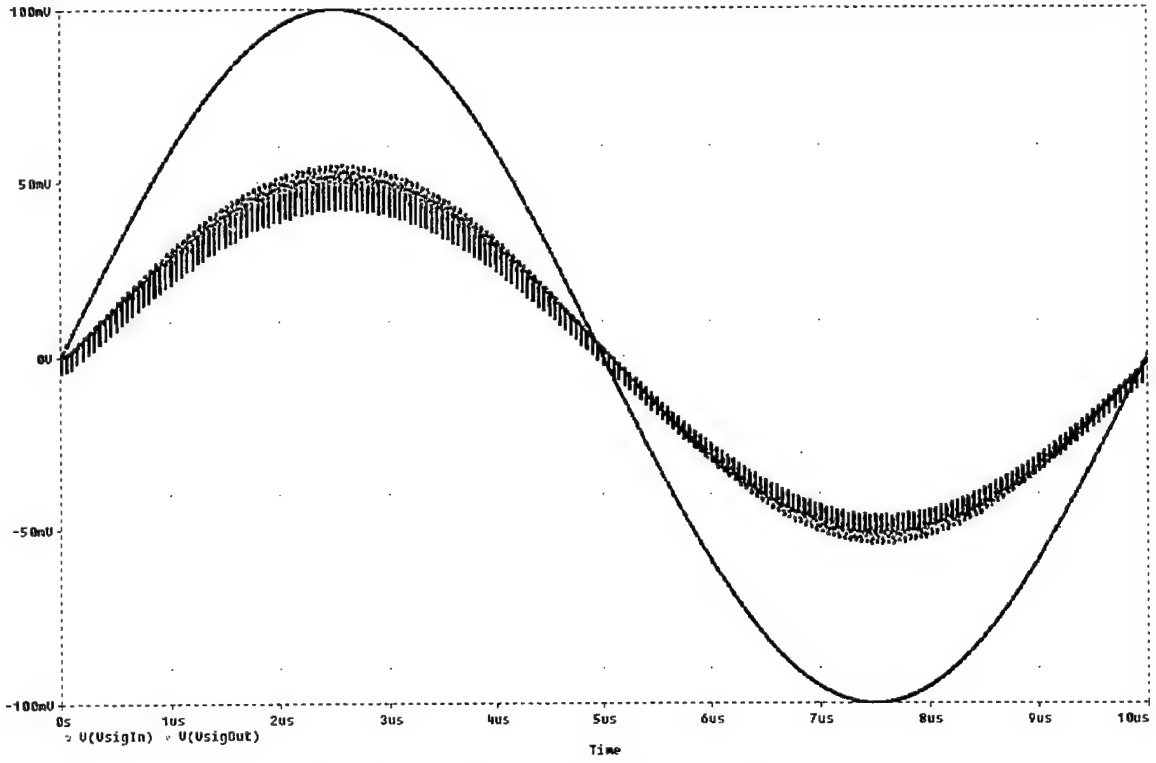

Figure 7.6: Output of 12315 Ω Floating Bilinear Resistor.

basic FBRs in the filter. Figure 7.6 shows simulation results obtained by placing a FBR in series with a standard 12315 Ω resistor and measuring the voltage at their connection node. The 100 mV amplitude, 100 kHz sine wave is the input. The signal at 50 mV is the output node of the FBR. This verifies size and operation of the FBR. Simulations were also conducted with DC and 1 MHz signals showing similar results. The variable FBR was also tested in this manner and produced values of 9850 Ω, 12315 Ω, 24630 Ω, 36945 Ω, 49260 Ω, and 61575 Ω as predicted.

E. OPERATIONAL AMPLIFIERS

The operational amplifier design is shown in Figure 7.7. Performance results

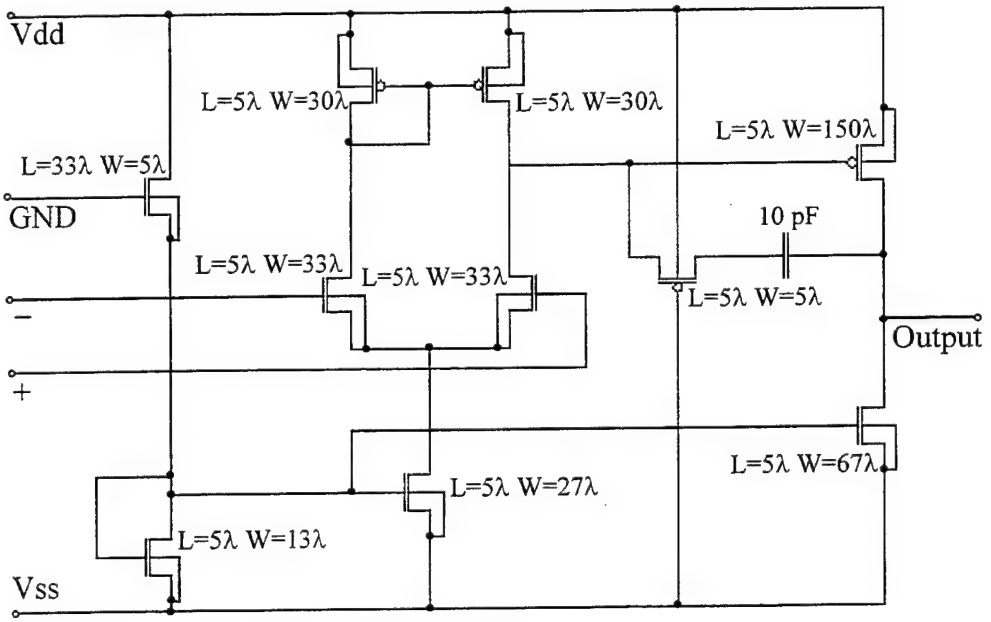

Figure 7.7: Operational Amplifier Schematic.

are calculated from data shown in Figure 7.8 and Figure 7.9. DC gain for the op amp was found to be 106.6 dB. The 3 dB corner frequency, brought about by the compensating capacitor pole, is 12.35 Hz. This provides a Gain Bandwidth Product of 2.65 MHz. The zero dB crossing point is at 64 MHz due to the zero at approximately 2 MHz extending

the region of positive gain, while the first parasitic pole does not appear until about 40 MHz. The phase margin was found to be 61°.

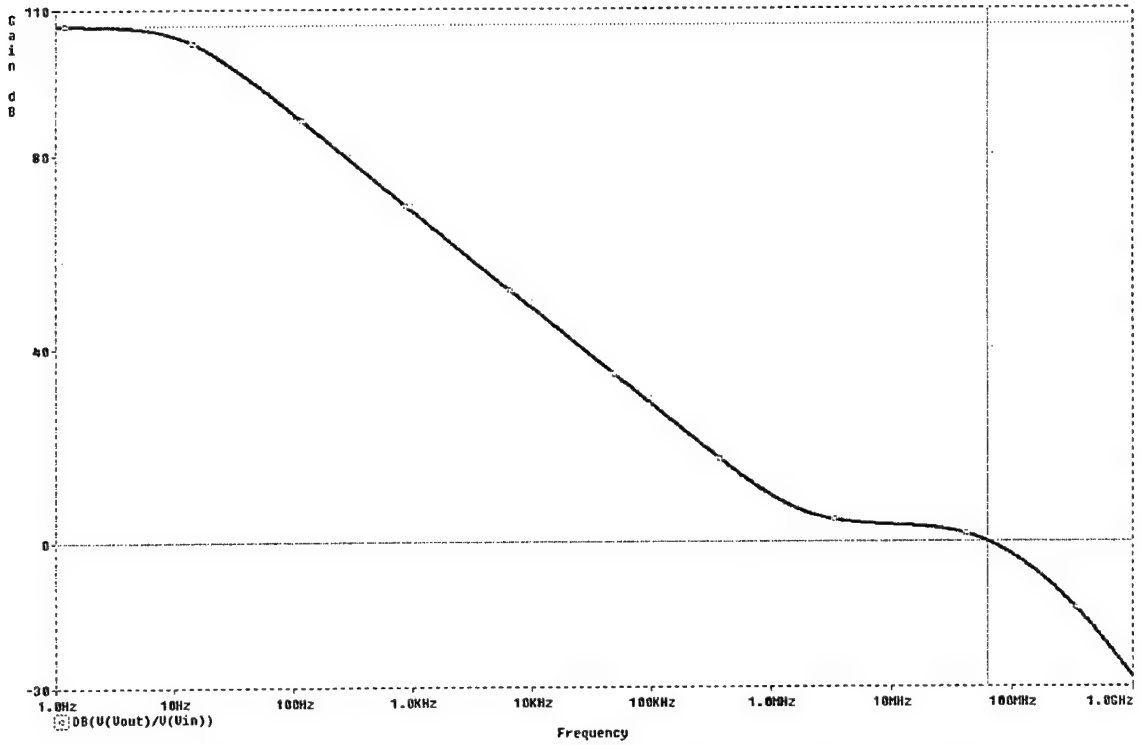

Figure 7.8: Operational Amplifier Gain Frequency Response.

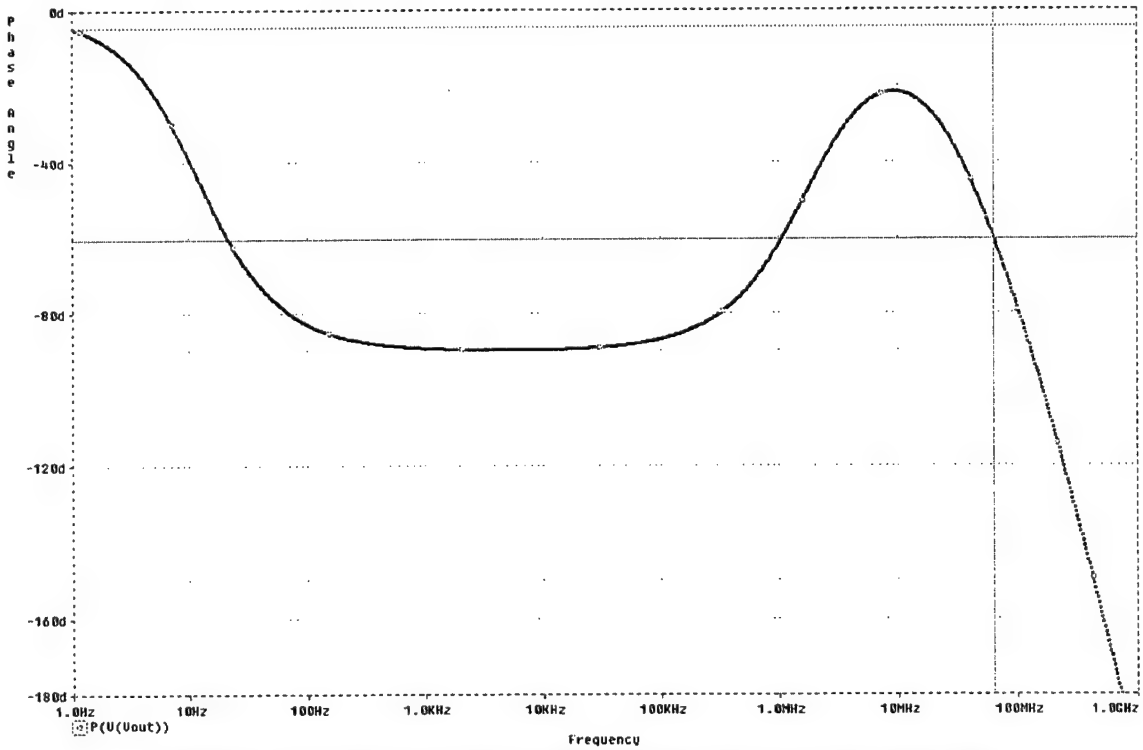

Figure 7.9: Operational Amplifier Phase Frequency Response.

The op amp design provides suitable performance for operation of the filter at frequencies up to 1 MHz, with some operational capability for signals beyond 1 MHz.

F. LOGIC SECTIONS

Schematic designs from Chapter VI were converted to transistor level schematics using basic component blocks and interconnecting them. All logic is combinatorial, so varying selection bit inputs from high to low was the only testing required. All logic performed according to the truth tables in Chapter VI.

G. OVERALL CHIP

The layout of the chip needed to conform to a standard size *Tiny Chip* of 2.25 mm by 2.22 mm and 40 pads. The chip layout area is 2.15 mm by 2.15 mm and it uses 40 pads. Figure 7.10 shows the circuit floor plan which is the location of functional blocks and pads, while Table 7.2 explains the function of each pad. For this prototype chip, a design decision was made to include test structures for each functional block to facilitate chip testing when fabrication is complete. The area and pads available on the chip would alternately allow placing two independent GIC filters, and two independent op amps in future designs once prototype testing is complete.

Frequency response analysis was conducted in PSPICE. All possible filter combinations were simulated. Resulting charts are contained in Appendix B. These charts are for a 10 MHz clock.

The chip design has been submitted to MOSIS for fabrication. Five chips packaged in 40 pin *Dual Inline Packages* (DIPs) have been ordered for testing.

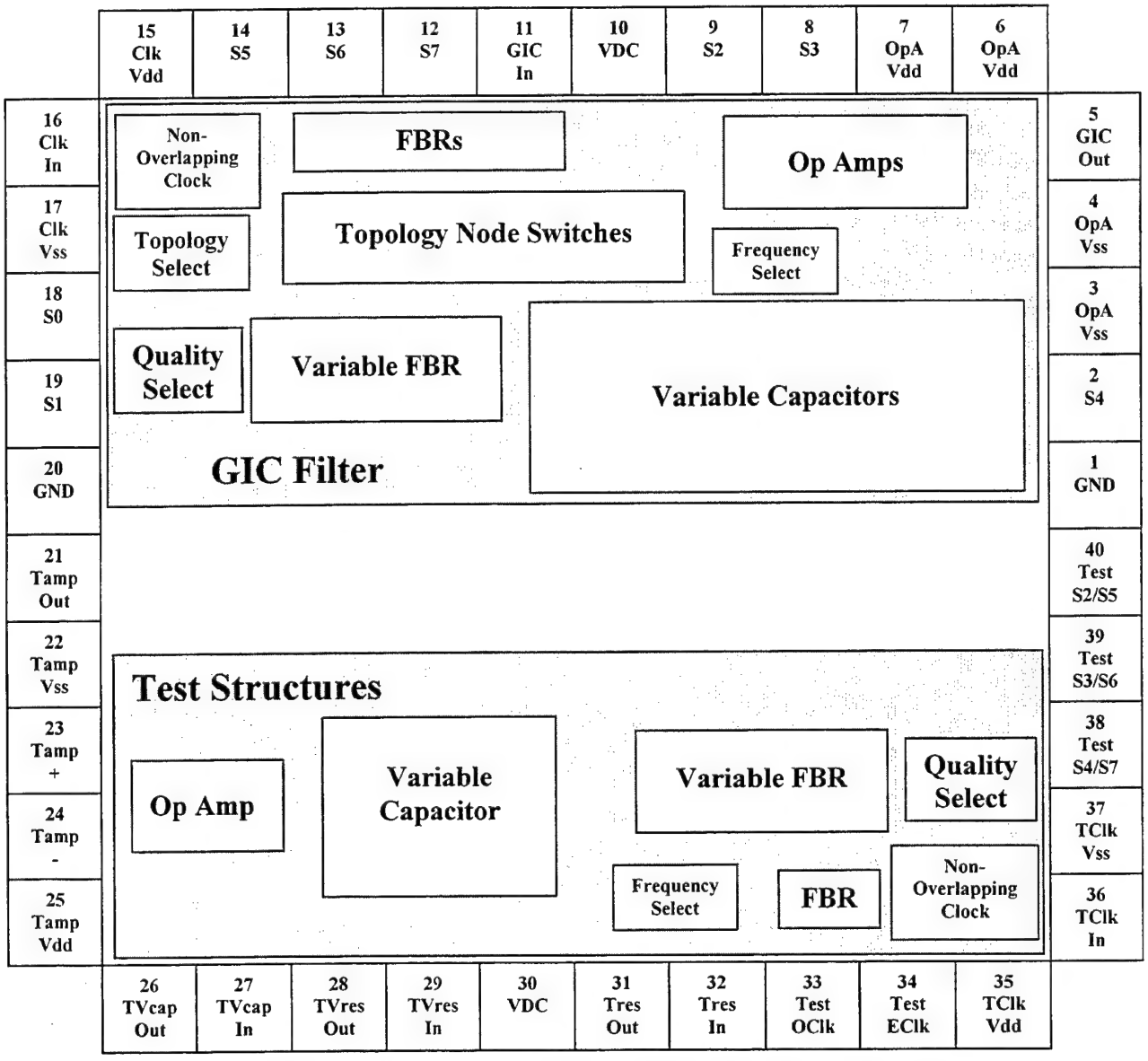

Figure 7.10: Chip Functional Block and Pad Locations.

Pad	Function
GND (1, 20)	Chip Ground
VDC (10, 30)	Power for Logic Blocks (+5 V)
OpA Vss (3, 4)	Op Amp Negative Power (-5 V)
OpA Vdd (6, 7)	Op Amp Positive Power (+5 V)
Clk Vss (17)	Non-Overlapping Clock Negative Power (-5 V)
Clk Vdd (15)	Non-Overlapping Clock Positive Power (+5 V)
Clk In (16)	Clock Input for GIC Filter
GIC Out (5)	Output Signal from GIC Filter
GIC In (11)	Input Signal to GIC Filter
S0-S1 (18, 19)	Topology Selection Bits for GIC Filter
S2-S4 (9, 8, 2)	Frequency Selection Bits for GIC Filter
S5-S7 (14, 13, 12)	Quality Factor Selection Bits for GIC Filter
Tamp Vss (22)	Test Op Amp Negative Power (-5 V)
Tamp Vdd (25)	Test Op Amp Positive Power (+5 V)
TClk Vss (37)	Test Non-Overlapping Clock Negative Power (-5 V)
TClk Vdd (35)	Test Non-Overlapping Clock Positive Power (+5 V)
Tamp + (23)	Test Op Amp Non-Inverting Terminal
Tamp - (24)	Test Op Amp Inverting Terminal
Tamp Out (21)	Test Op Amp Output Terminal
TVcap In (27)	Test Variable Capacitor Input Node
TVcap Out (26)	Test Variable Capacitor Output Node
TVres In (29)	Test Variable Floating Bilinear Resistor Input Node
TVres Out (28)	Test Variable Floating Bilinear Resistor Output Node
Tres In (32)	Test Floating Bilinear Resistor Input Node
Tres Out (31)	Test Floating Bilinear Resistor Output Node
TClk In (36)	Test Non-Overlapping Clock Input
Test OClk (33)	Test Non-Overlapping Clock Odd Clock Signal
Test EClk (34)	Test Non-Overlapping Clock Even Clock Signal
S2/5-S4/7 (40, 39, 38)	Selection Bits for Test Variable FBR and Test Variable Capacitor

Table 7.2: Pad Functions

VIII. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

The project goal was to design, and submit for fabrication, a completed VLSI layout for a Digitally Programmable Analog VLSI GIC Filter. A filter of this design could be mass-produced using modern IC techniques, while still maintaining tight control of performance across multiple chips. The filter would have speed and simplicity advantages over a DSP filter by avoiding analog-to-digital conversion for processing and digital-to-analog conversion for output. Additionally, filtering is continuos, so there is no digital processing time lag. This project is a continuation of previous research into analog VLSI filters and has produced a completed layout for a prototype test chip that is being fabricated.

The basic circuit used for this filter was the GIC configuration. This technique utilizes inductor simulation, eliminating all the problems associated with the implementation of integrated inductors. Additionally, the GIC filter circuit exhibits all four basic filter topologies with minor relocation of component elements. Using a digital selection word allows function, frequency and quality factor changes to the filter by routing the signal through various passgates that change circuit topology. Replacing resistors (another difficult component in IC form) with switched capacitors gave the filter design the accuracy across chips needed for practical implementation.

The GIC filter was successfully designed, simulated and submitted for fabrication. Appendix B shows frequency response for all filter combinations. The responses show all four basic filter functions, eight selectable frequencies in a decade, and six selectable quality factors. The design provides further selectability through variation of the input

clock frequency. Lowering the clock frequency by one decade will shift all center frequencies lower by one decade. Desired frequency response is shown up to the design limit of 1 MHz. This prototype filter can operate for center frequencies near DC up to 1 MHz. More selectability could be added by increasing the bit size of the selection word. The two limiting factors on the bandwidth of this filter are the two phase non-overlapping clock and the operational amplifiers finite bandwidth. Using a Bi-CMOS (BJT and MOSFET) design or scaling to a VLSI technology with smaller gate lengths and higher MOSFET transconductance could further increase the filter bandwidth.

Appendix A shows VLSI mask layout representations used for circuit fabrication. Prototype chip design has been submitted and five chips have been ordered for continuation of this research.

B. RECOMMENDATIONS

This research has furthered previous research by converting a bread-board design to a silicon design and creating mask layouts for fabrication. The chip has been submitted for fabrication, so the next step in the research is testing of the prototype chip. Beyond testing, there are many areas of exploration for future work.

Bandwidth improvements, using the same fabrication process, could be made by designing a non-overlapping clock using bipolar logic and improving the operational amplifier frequency response by using a Bi-CMOS design. Scaling the design to state-of-the-art feature sizes could make further bandwidth improvements. Composite operational amplifiers may also improve the bandwidth.

There is reason to believe that this filter design might be highly insensitive to stray capacitance due to its GIC design. Further research into this area could be

conducted. Total dose radiation tolerance of the circuit is an additional research area that might show promising performance for this GIC filter. There are multiple areas that warrant future research on this design. Further refinements should be made to the prototype design for use in practical applications as well as research value.

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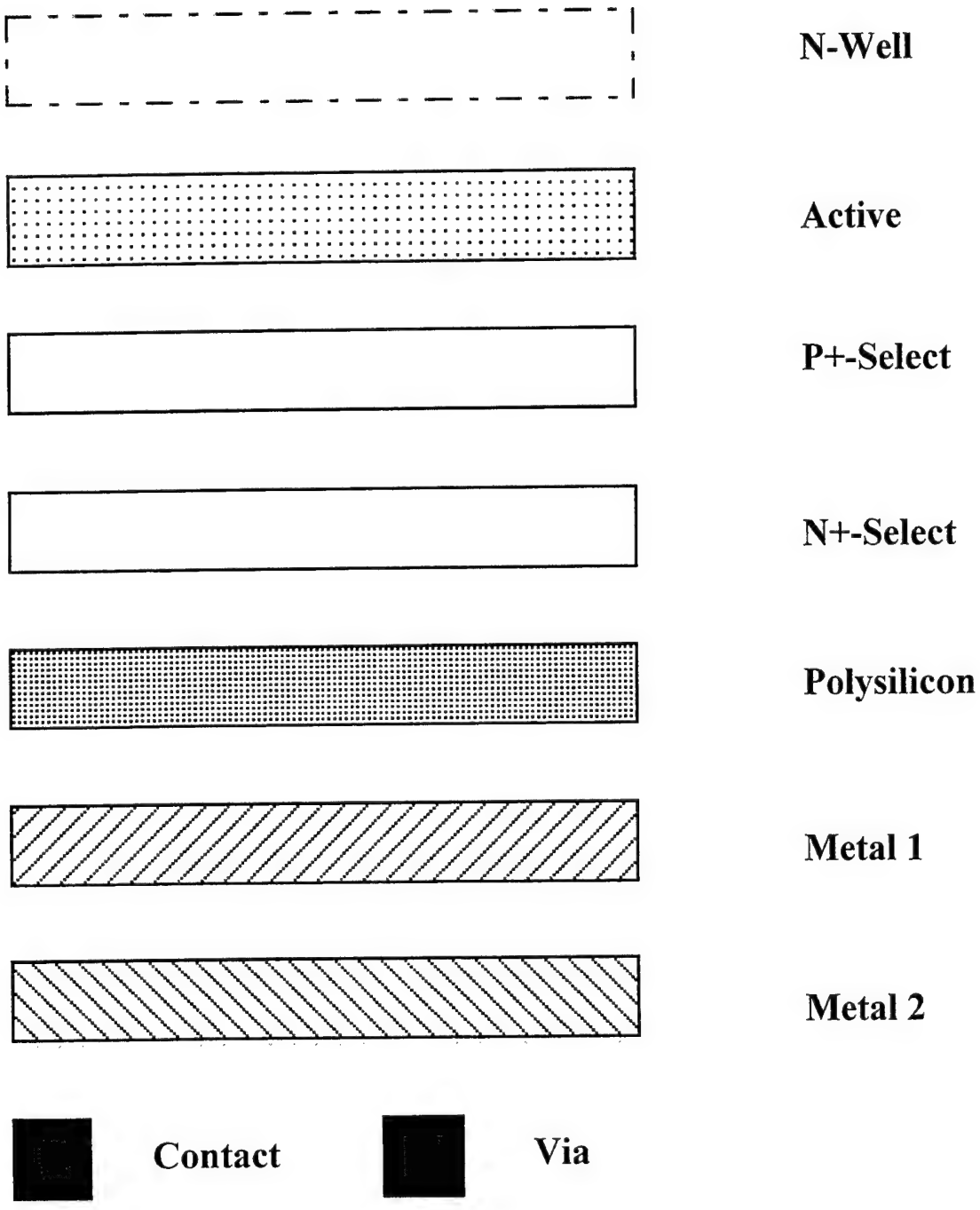
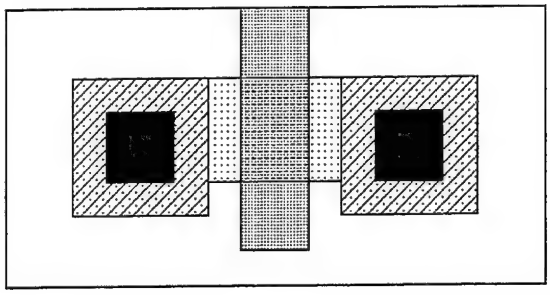
APPENDIX A. VLSI LAYOUT

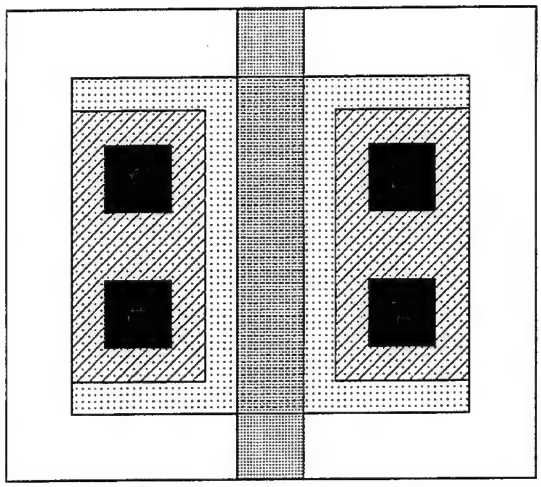
A. MASK LAYER PATTERNS



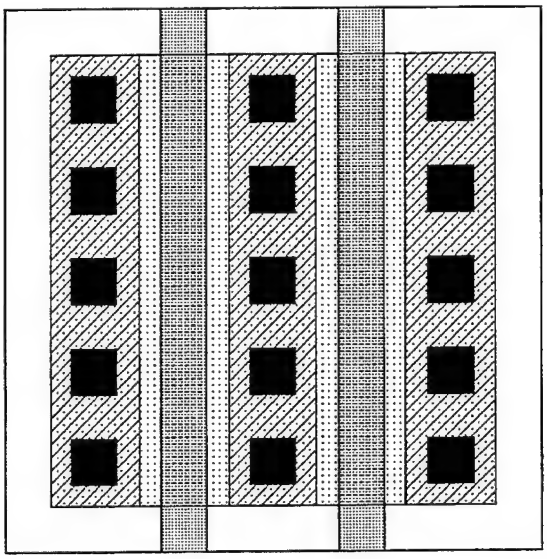
B. NFET (L=2λ W=3λ)



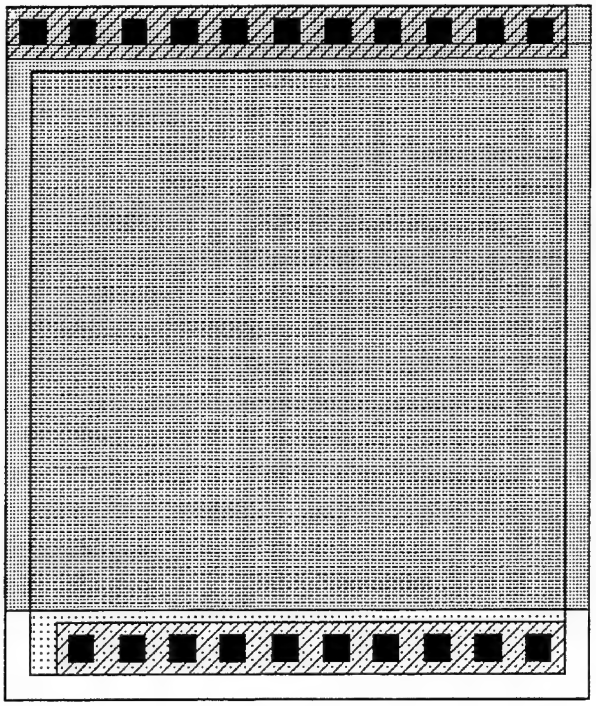
C. PFET (L=2λ W=10λ)



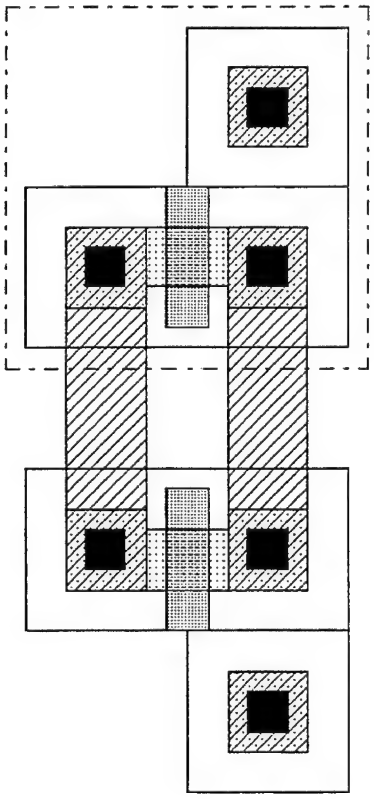
D. PFET (L=2λ W=40λ)



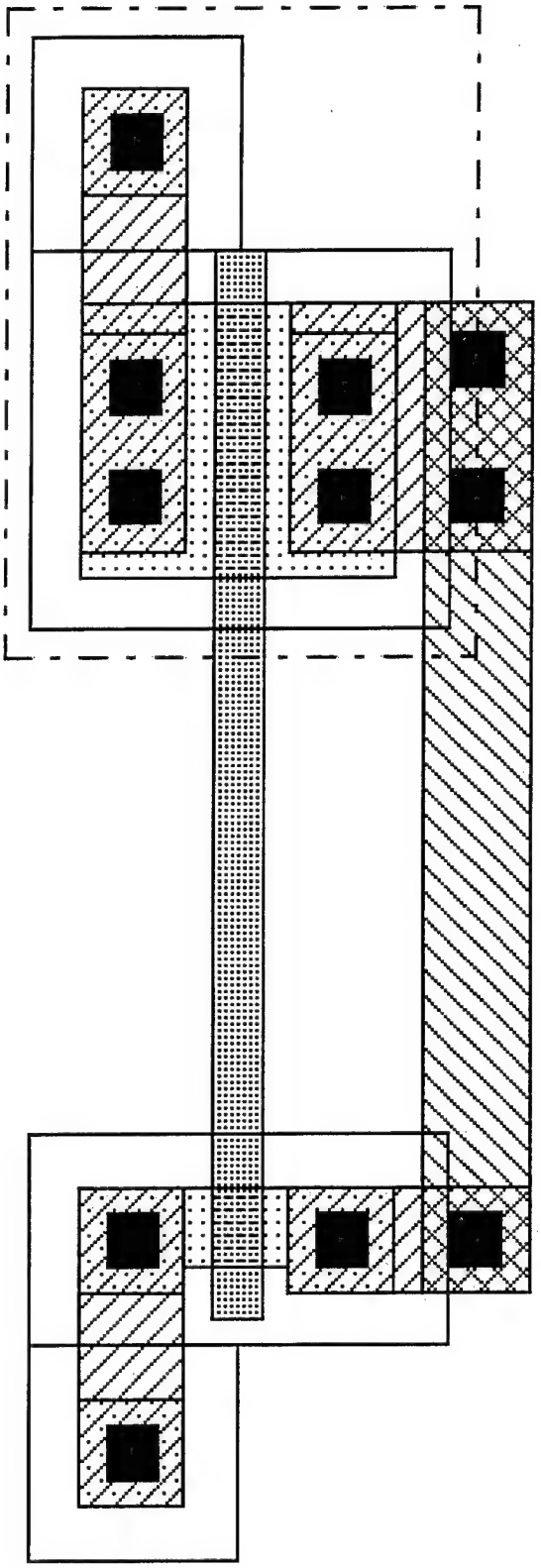
E. 2 PF CAPACITOR



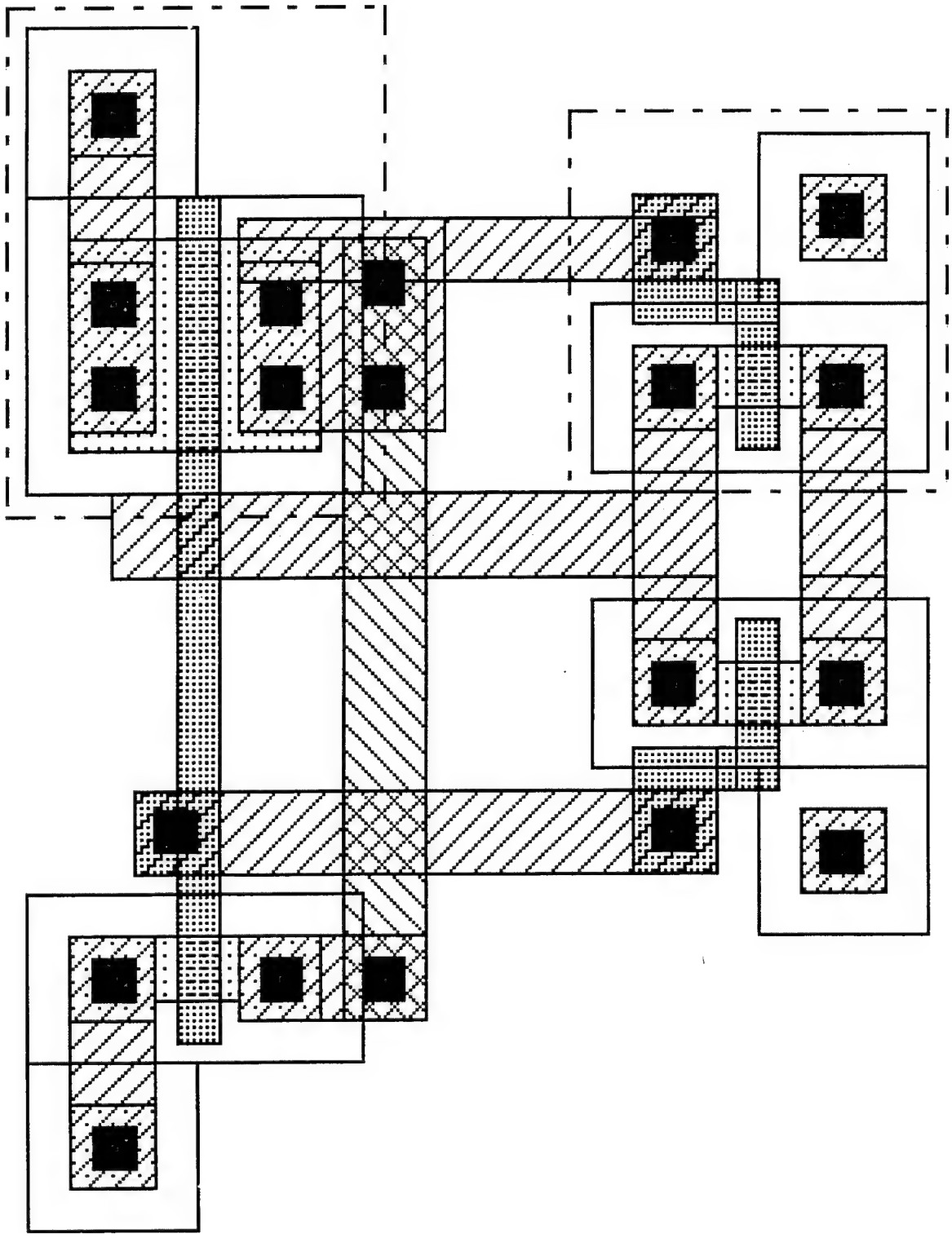
F. TWO-SIGNAL PASSGATE



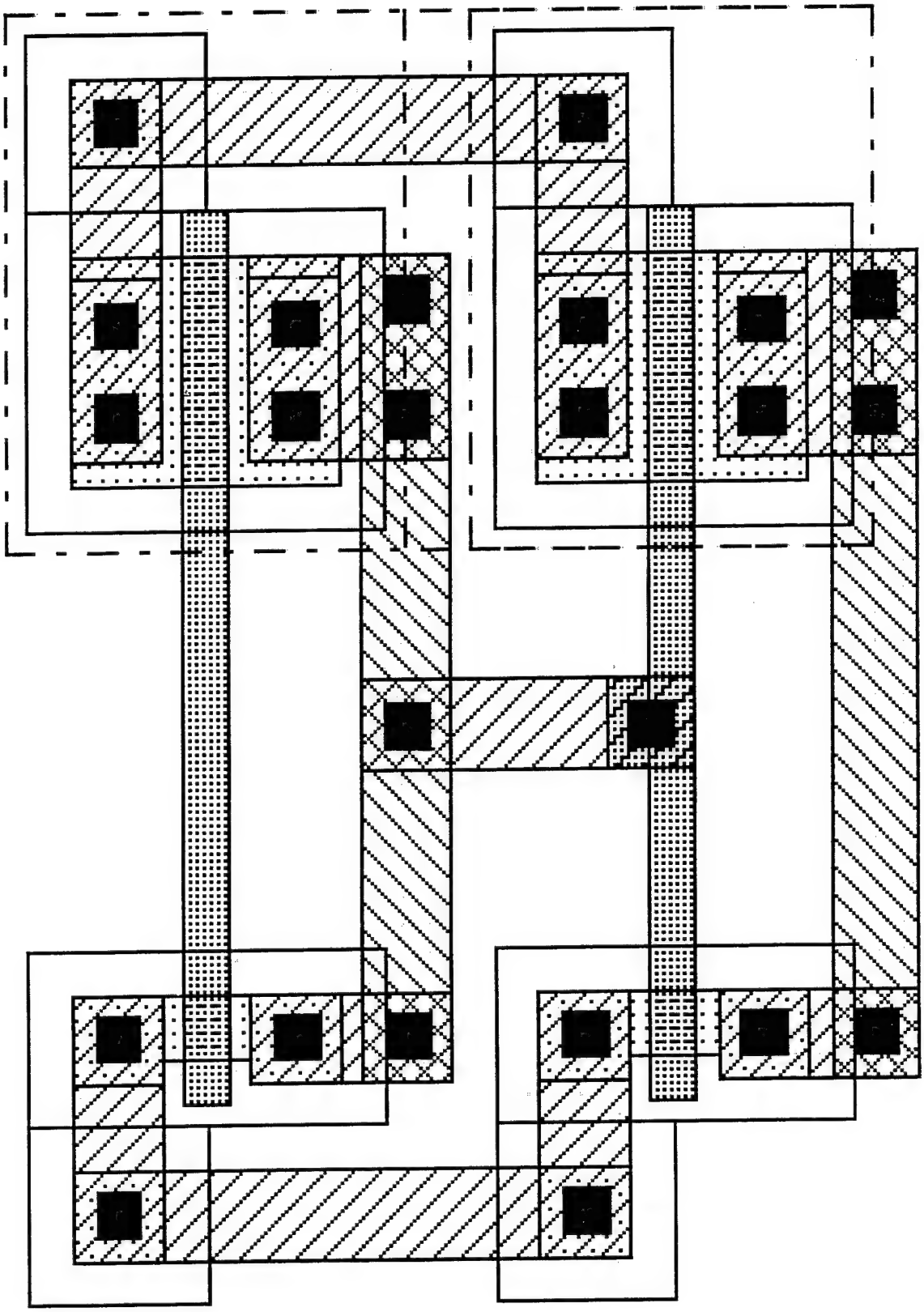
G. INVERTER



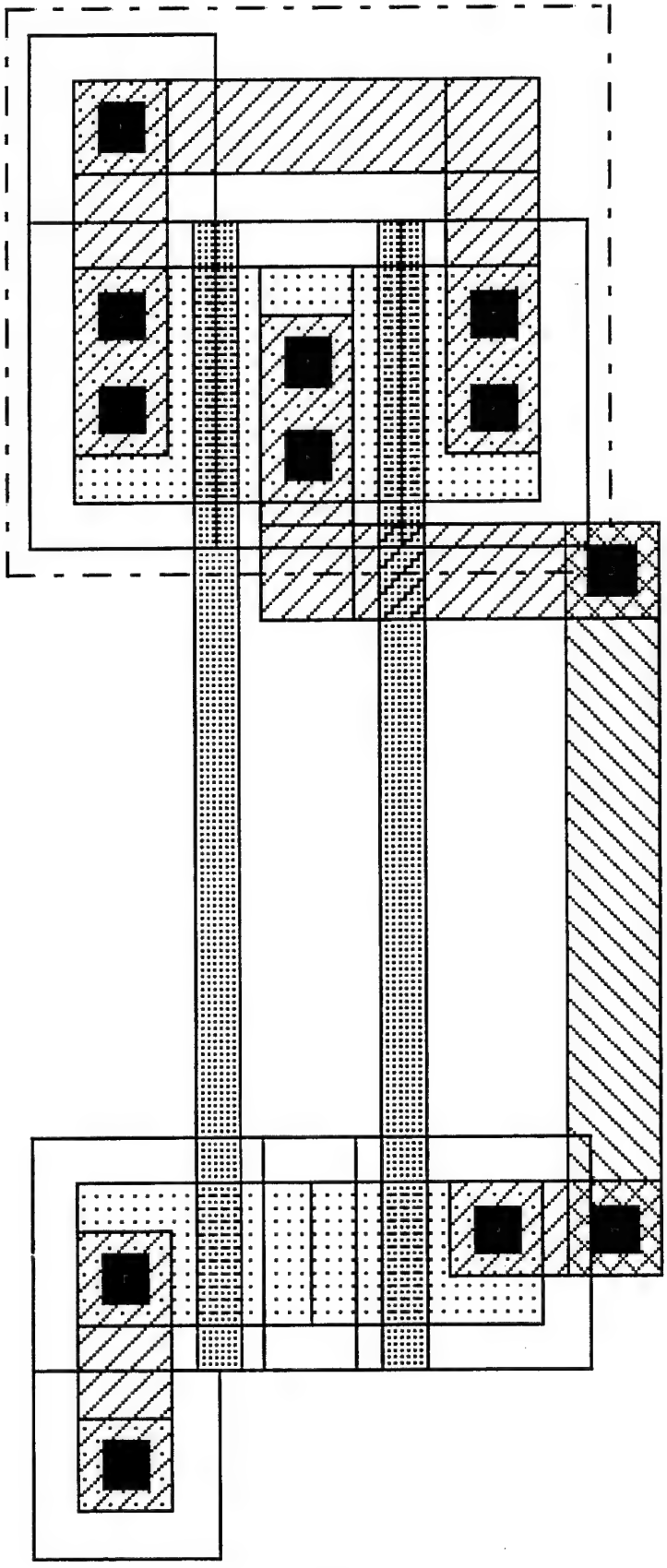
H. ONE-SIGNAL PASSGATE



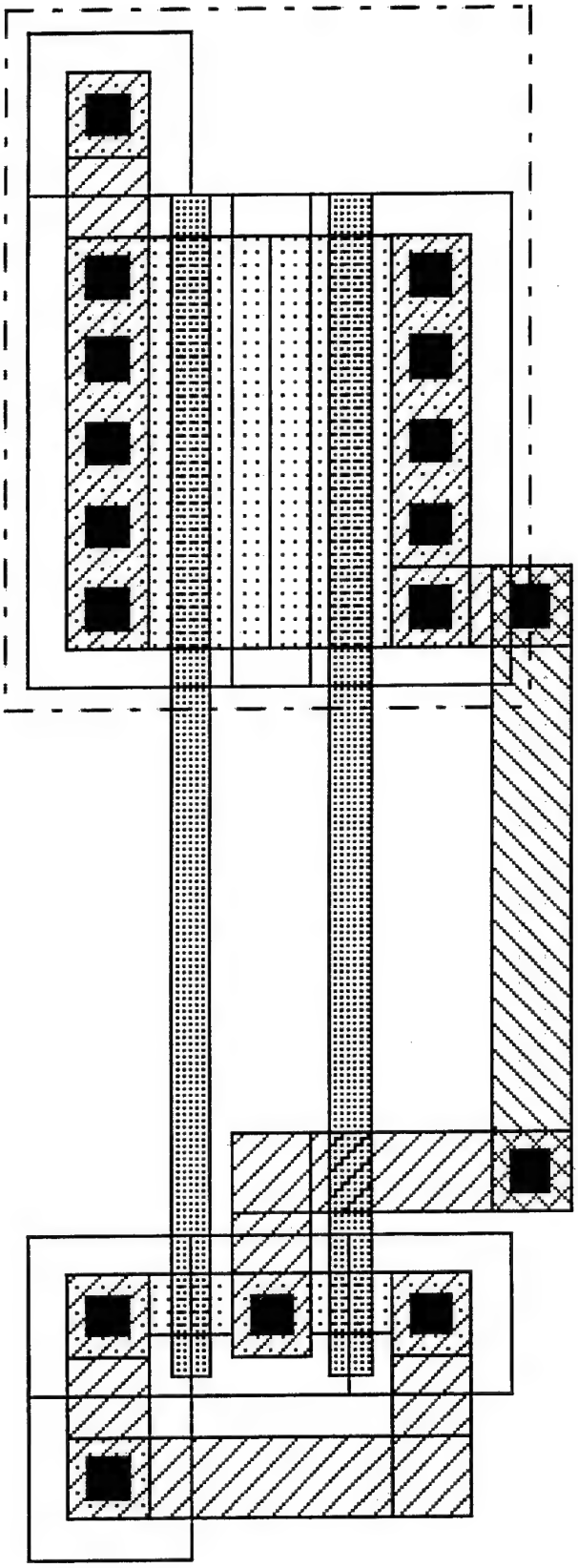
I. BUFFER



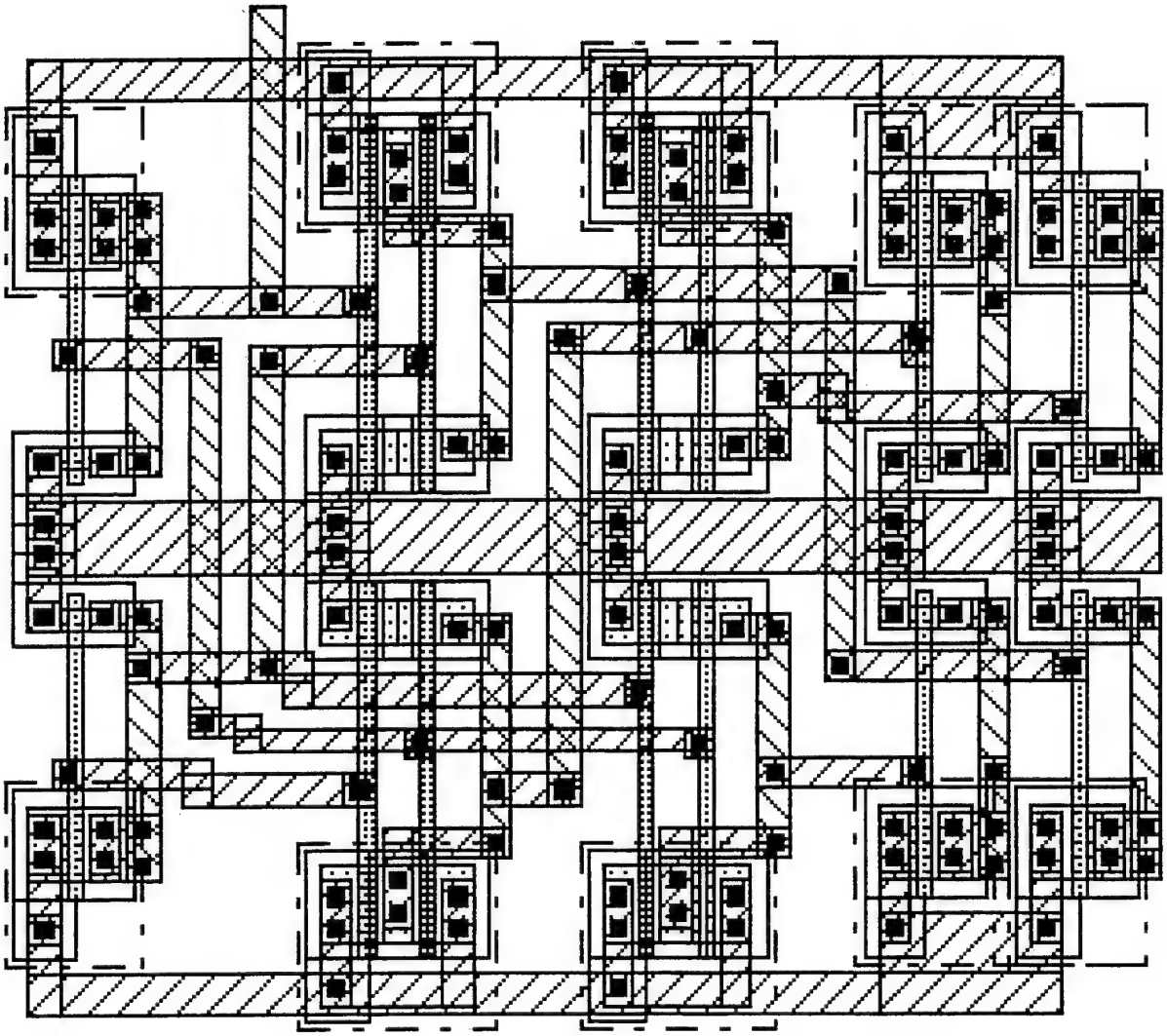
J. NAND GATE



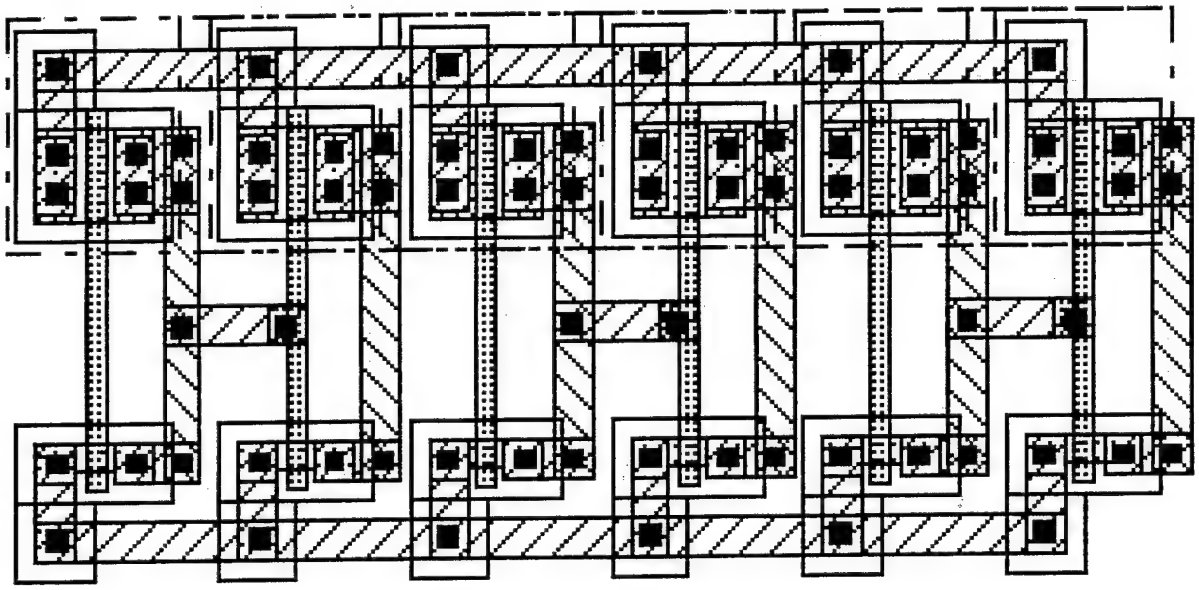
K. NOR GATE



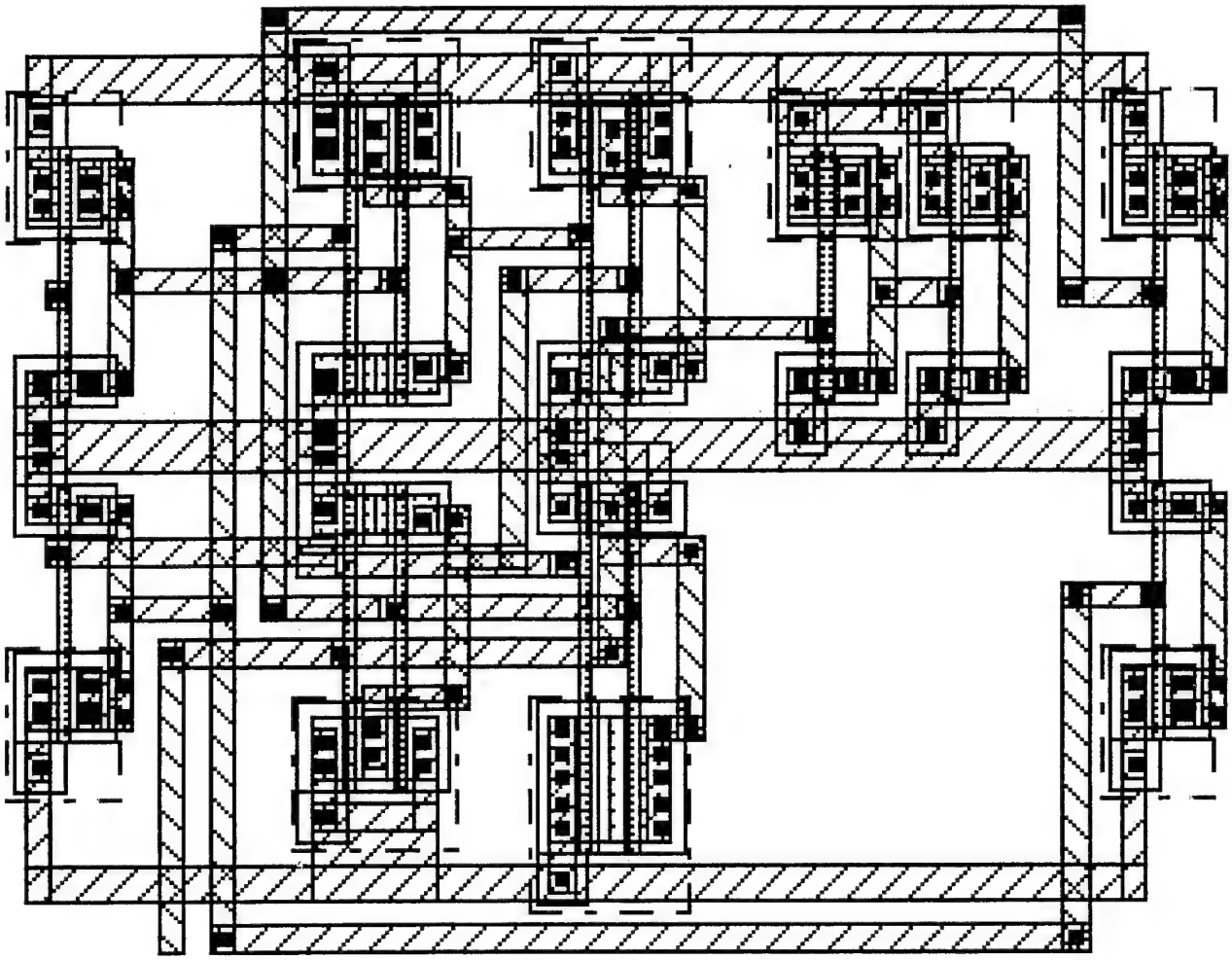
L. TOPOLOGY SELECTION



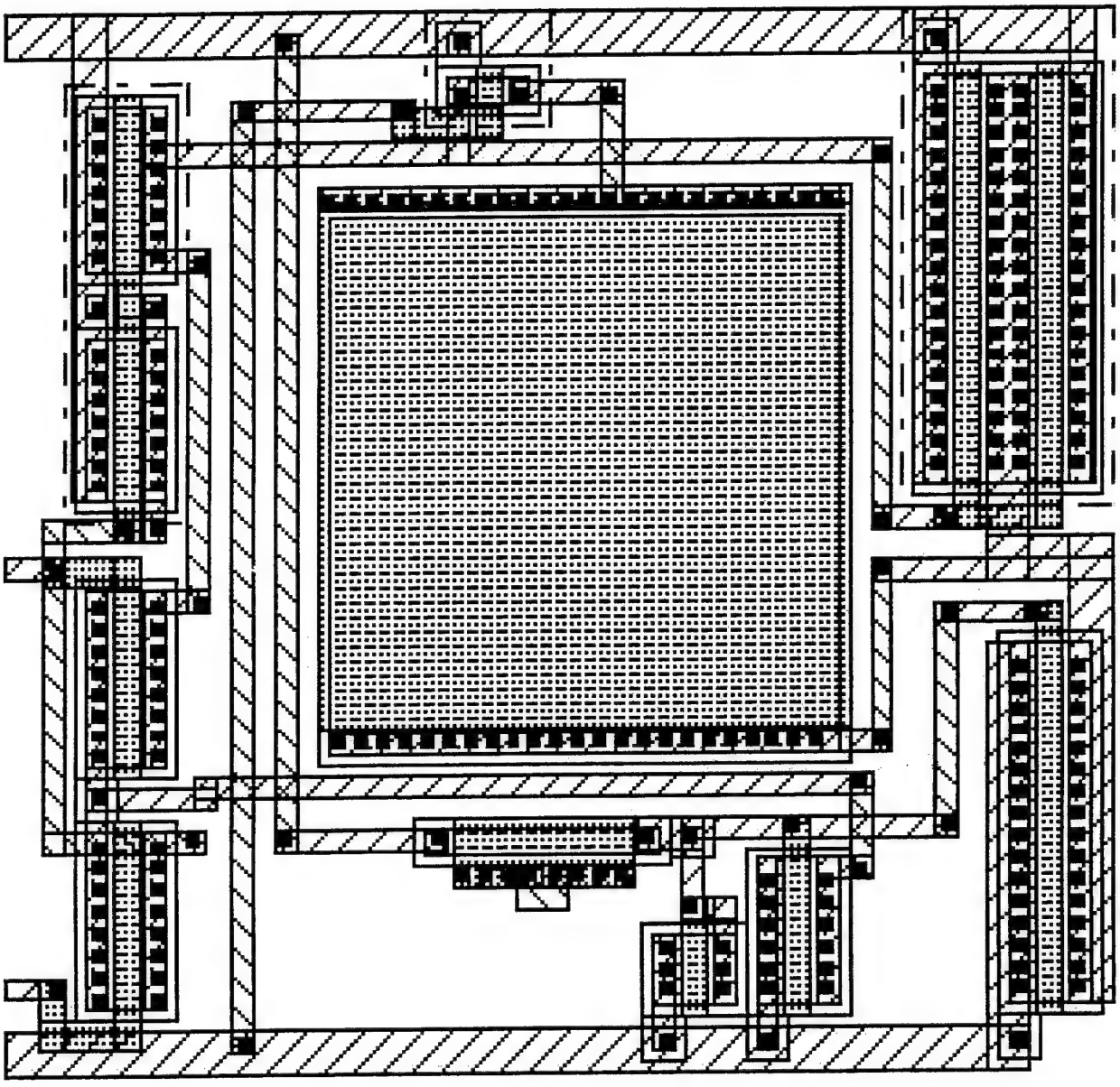
M. FREQUENCY SELECTION



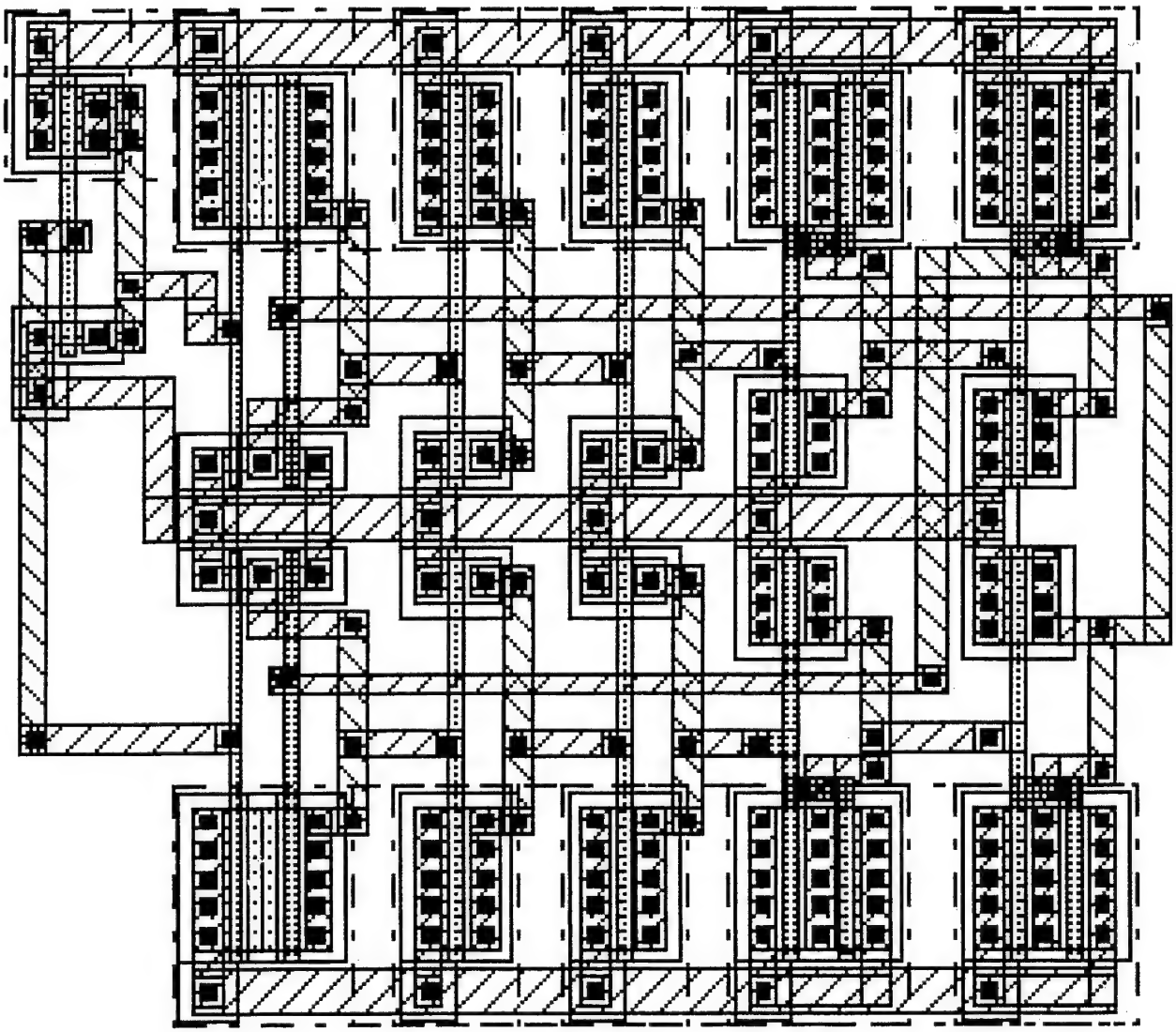
N. QUALITY FACTOR SELECTION



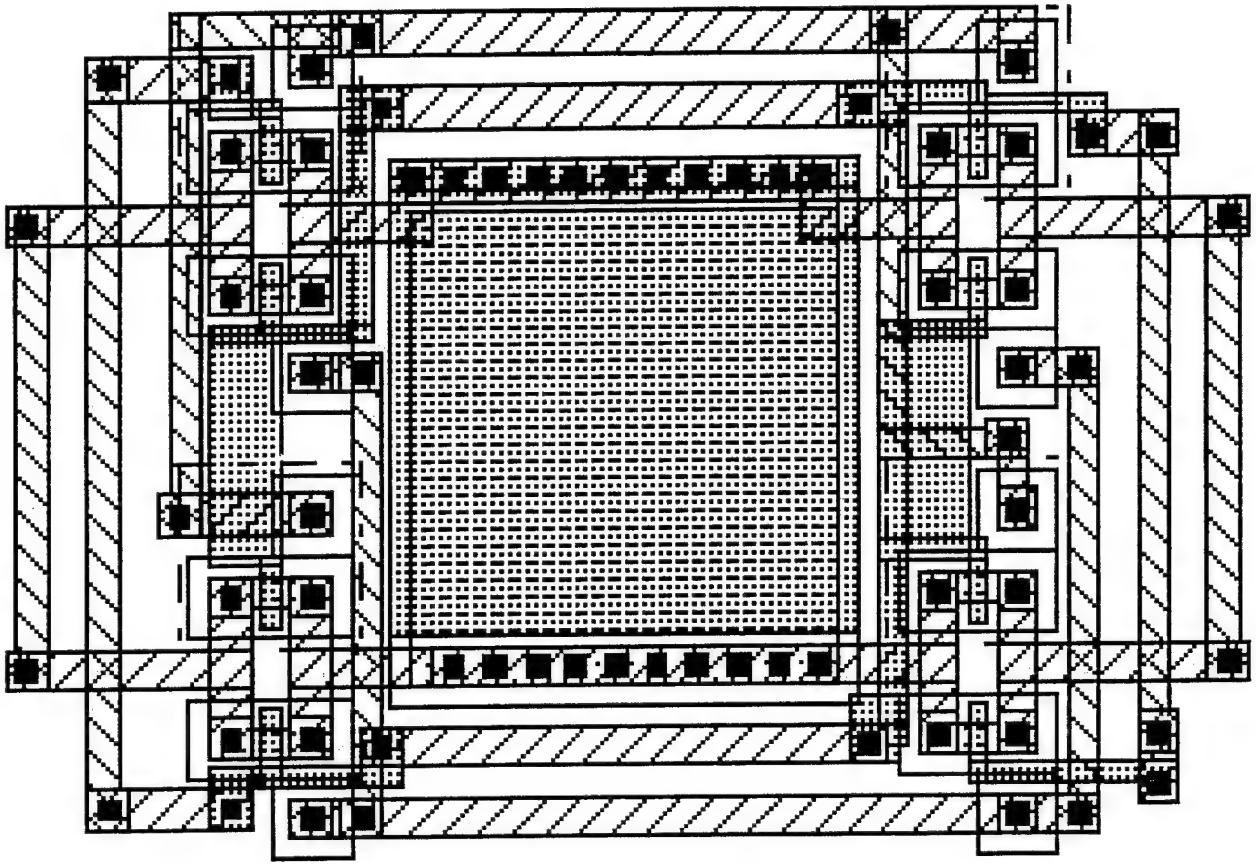
O. OPERATIONAL AMPLIFIER



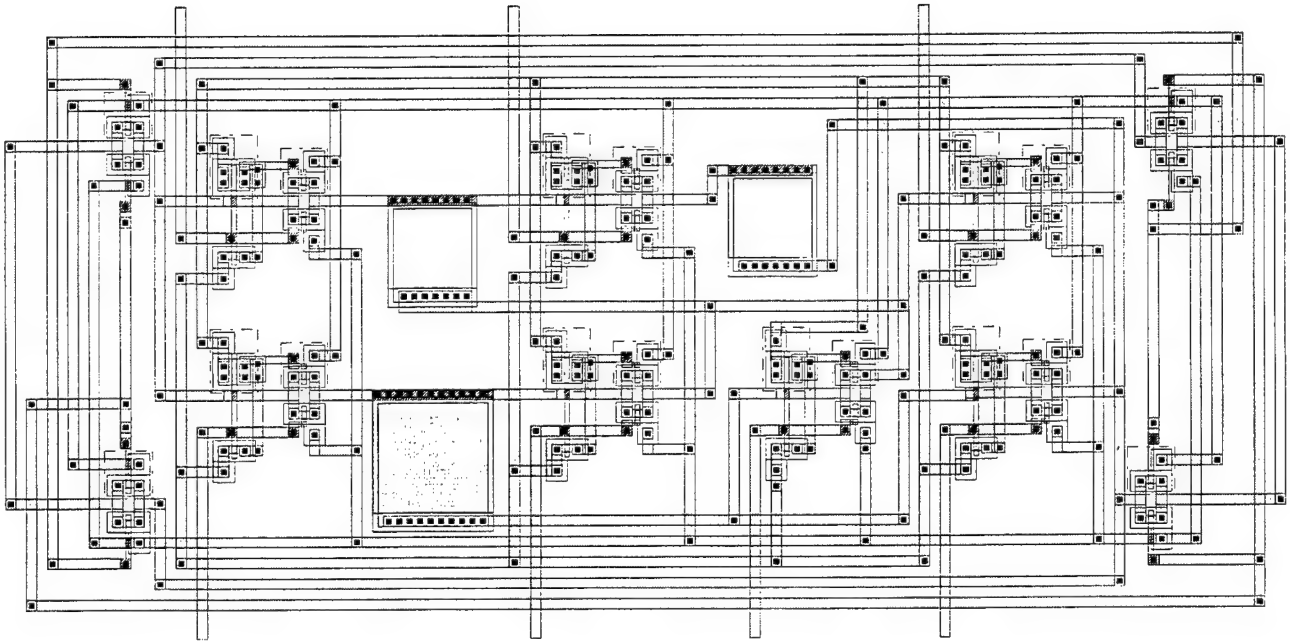
P. TWO PHASE NON-OVERLAPPING CLOCK



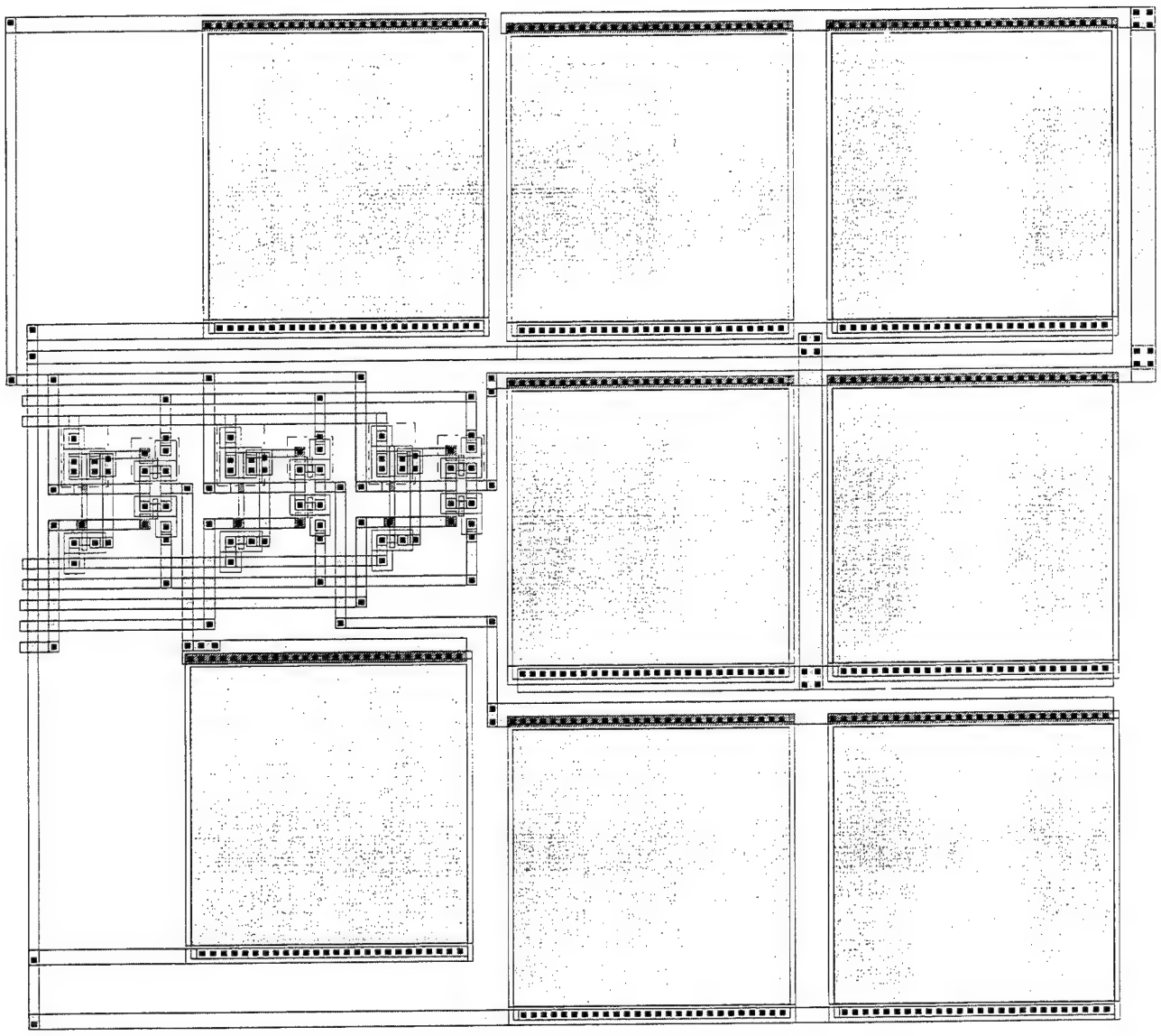
Q. FLOATING BILINEAR SWITCHED CAPACITOR RESISTOR



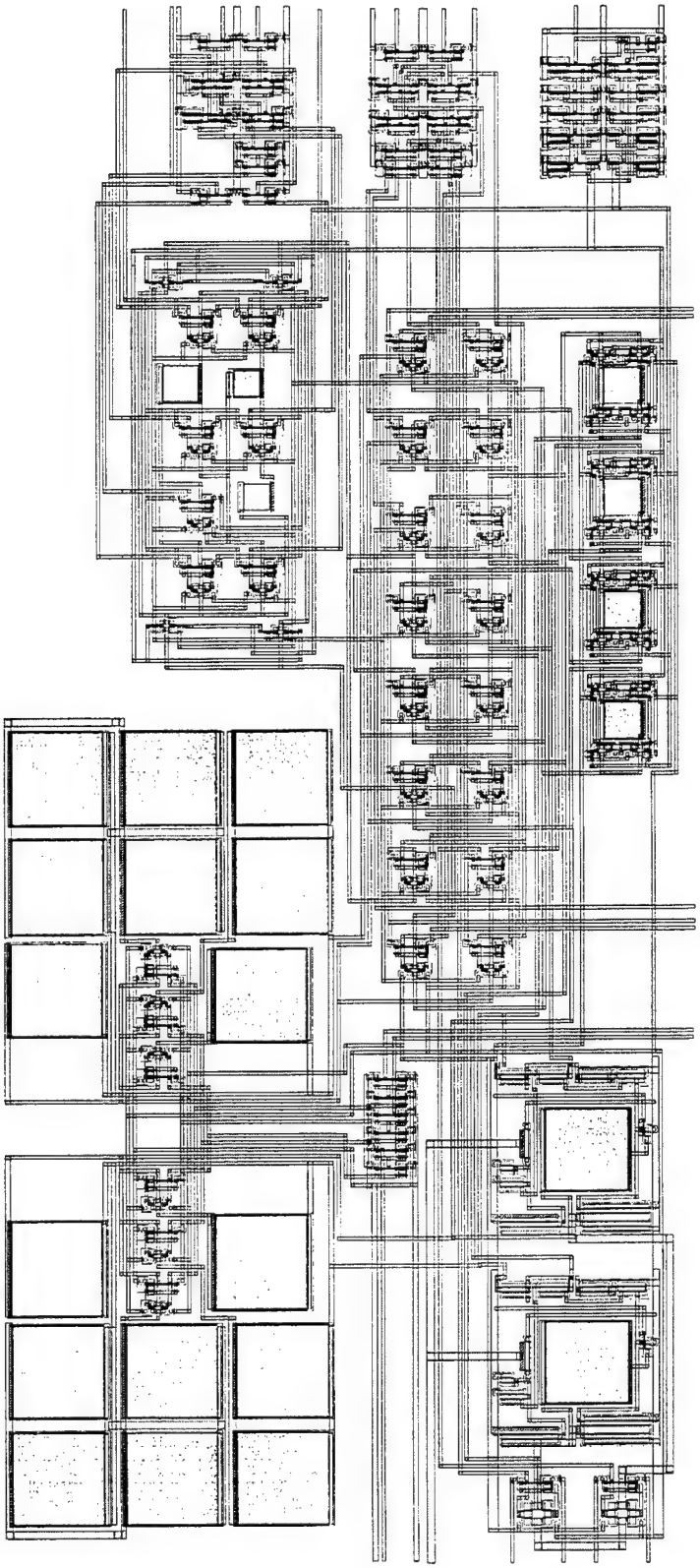
R. VARIABLE FLOATING BILINEAR RESISTOR



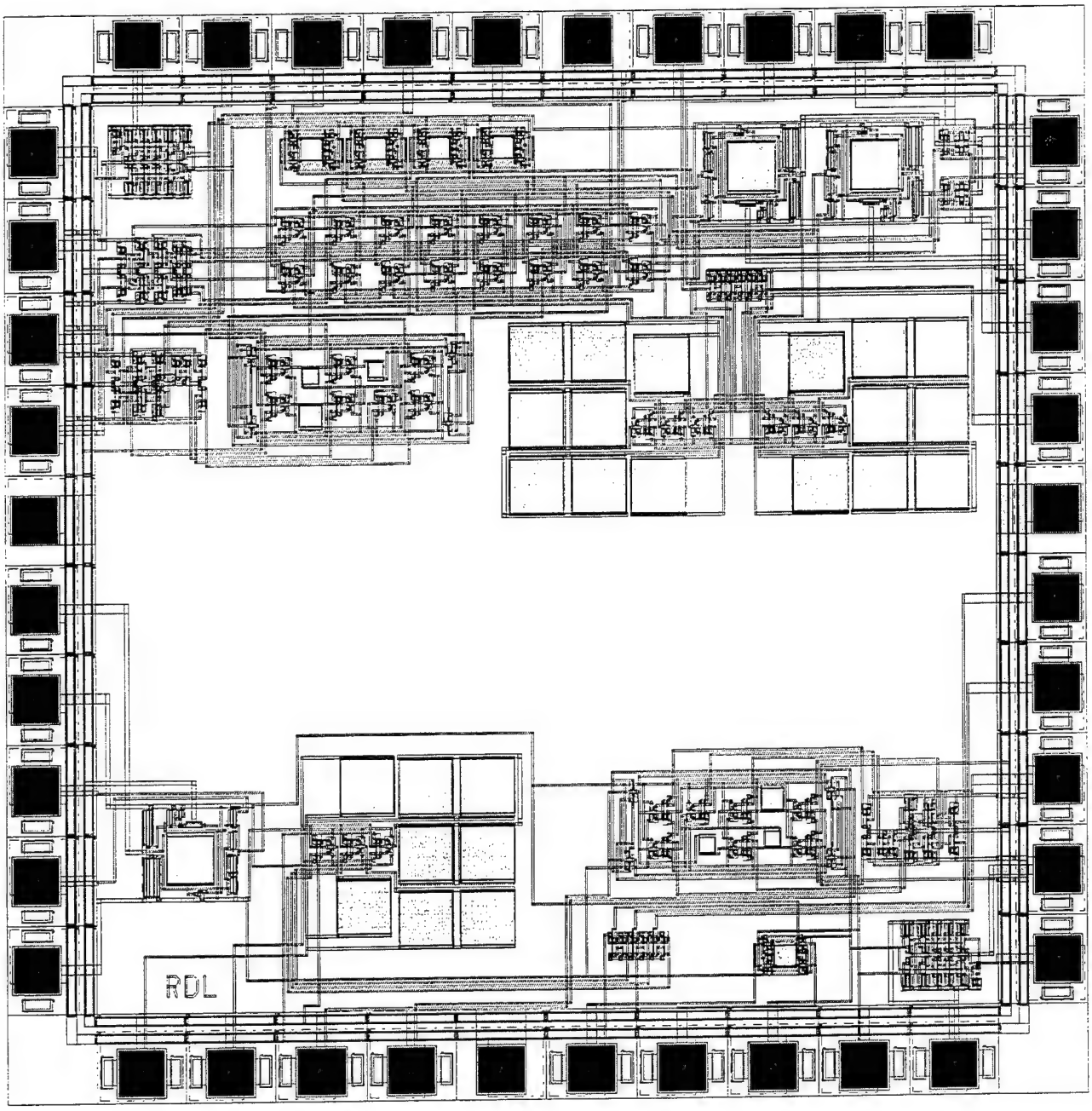
S. VARIABLE CAPACITOR



T. GENERALIZED IMPEDANCE CONVERTER FILTER



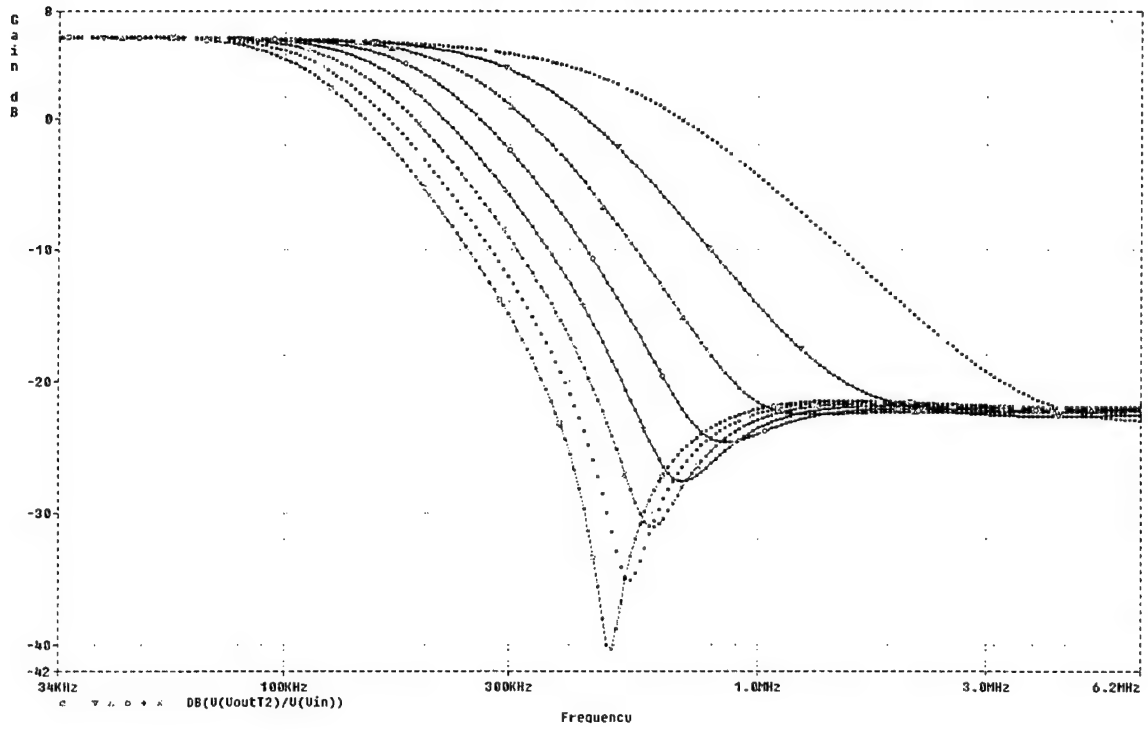
U. CHIP LAYOUT



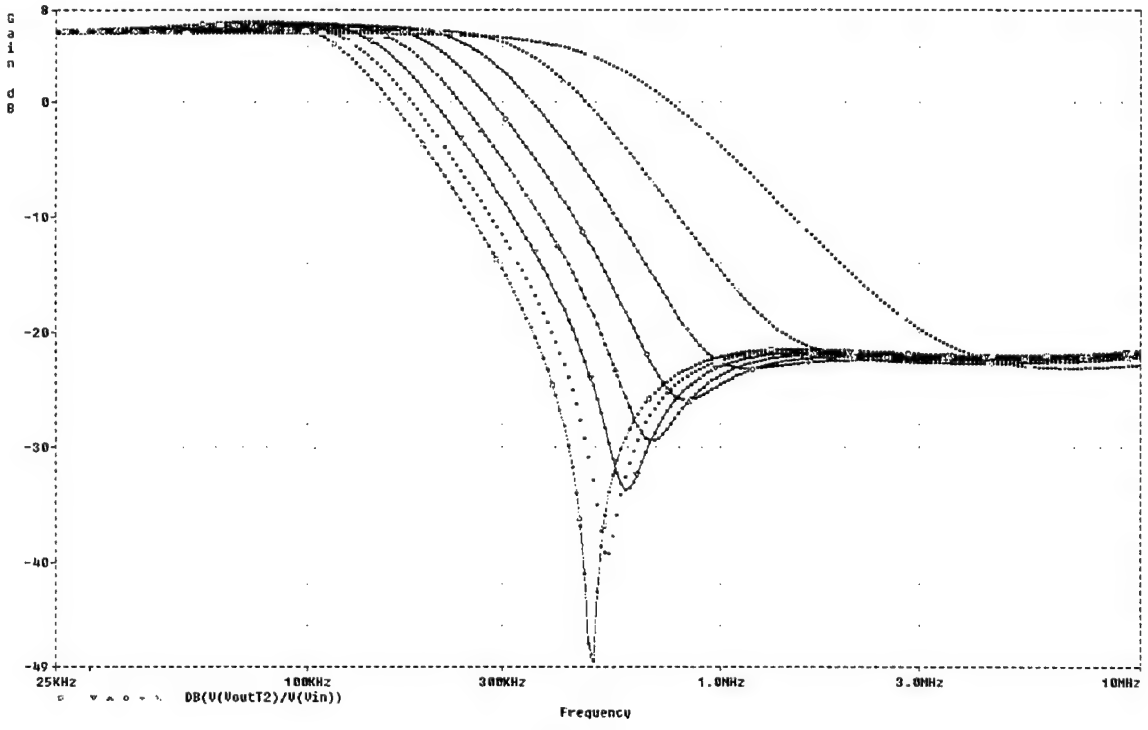
APPENDIX B. GIC FILTER MAGNITUDE RESPSONSE

A. LOW-PASS FILTER

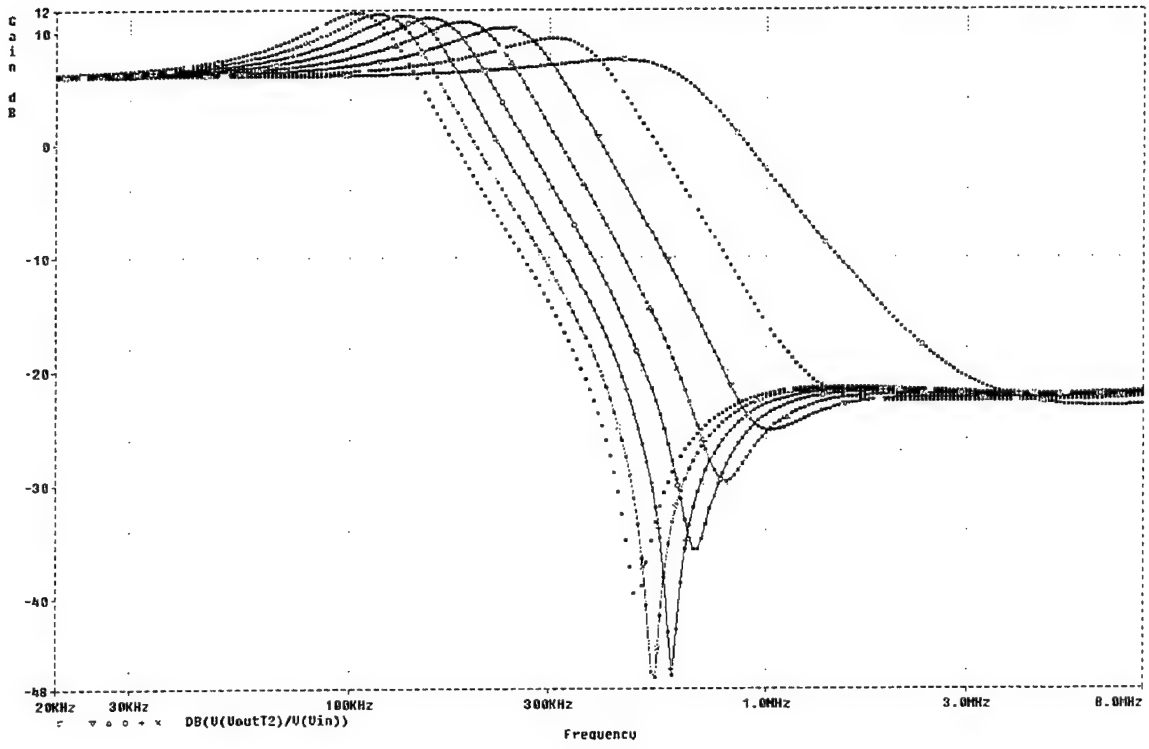
1. Low-Pass, Quality Factor = 0.8, All Frequencies



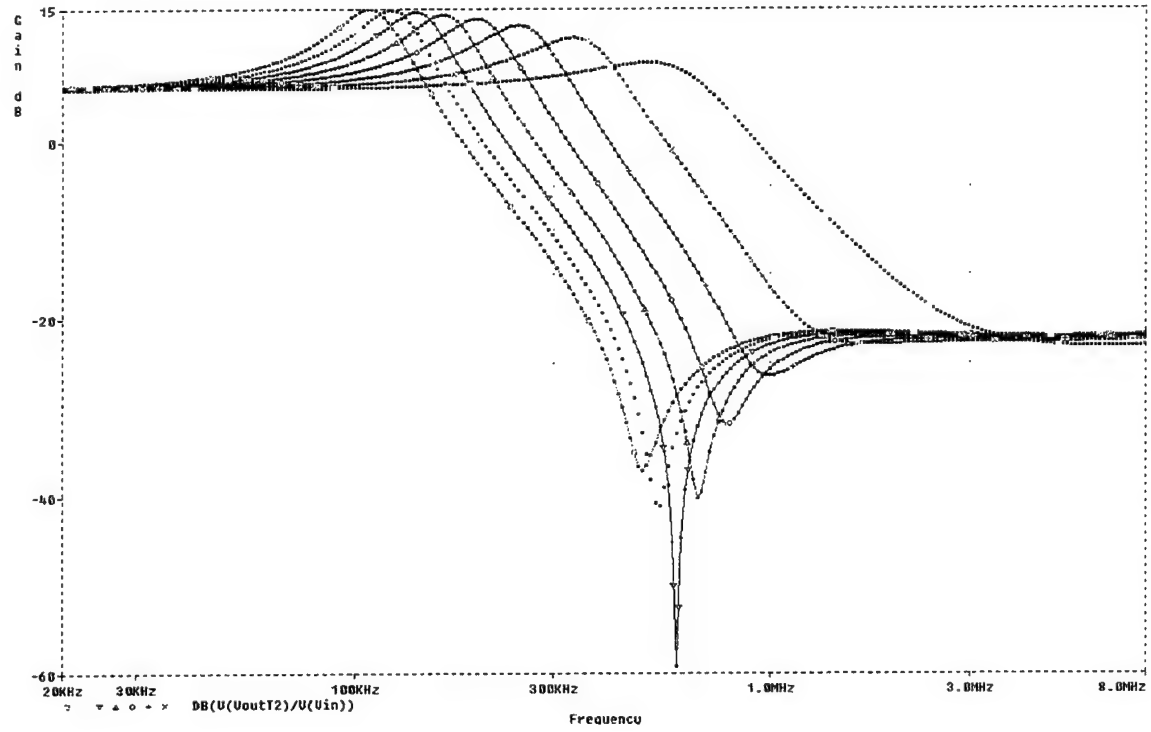
2. Low-Pass, Quality Factor = 1, All Frequencies



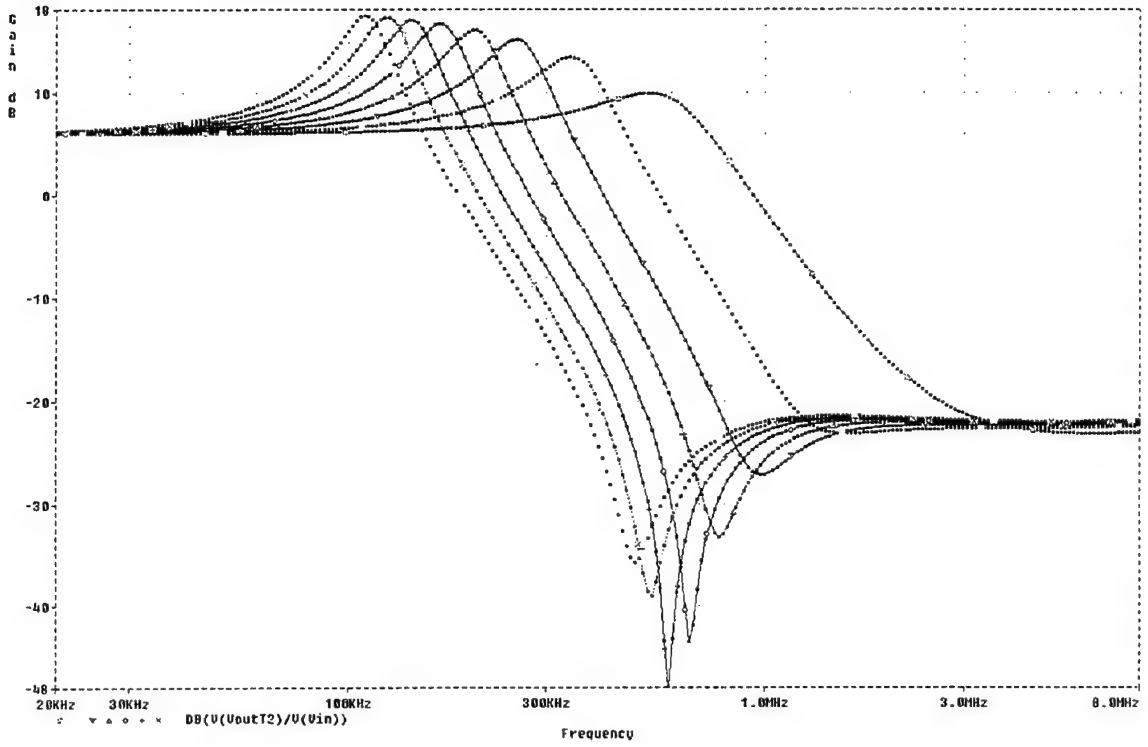
3. Low-Pass, Quality Factor = 2, All Frequencies



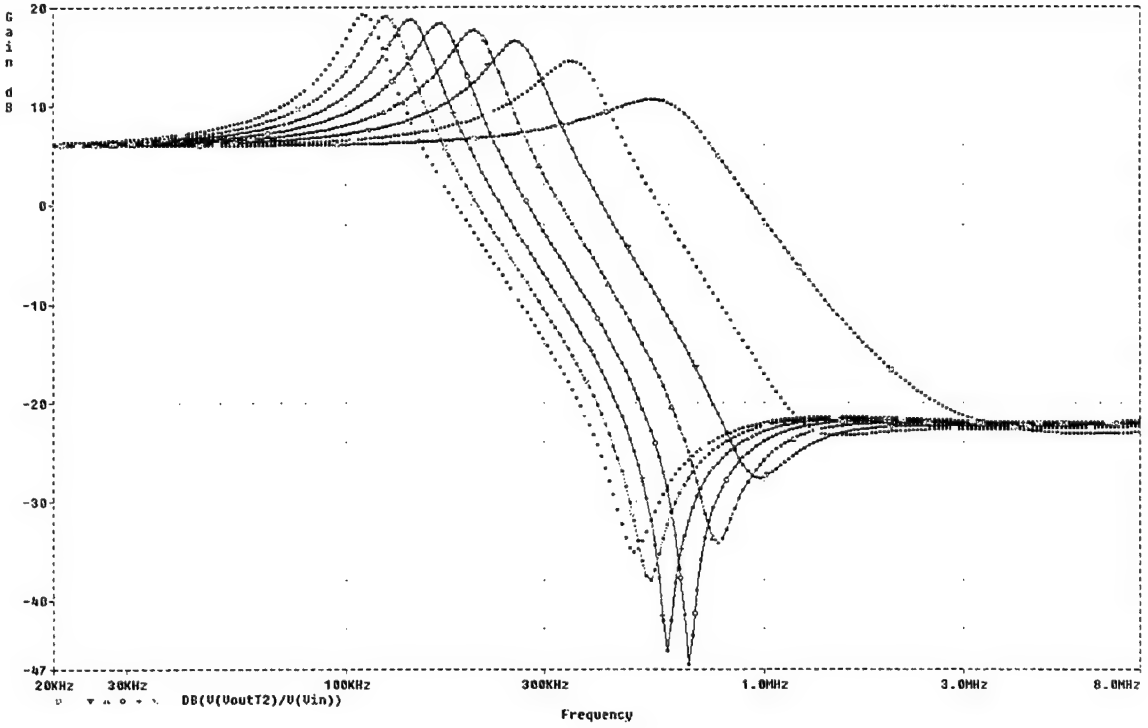
4. Low-Pass, Quality Factor = 3, All Frequencies



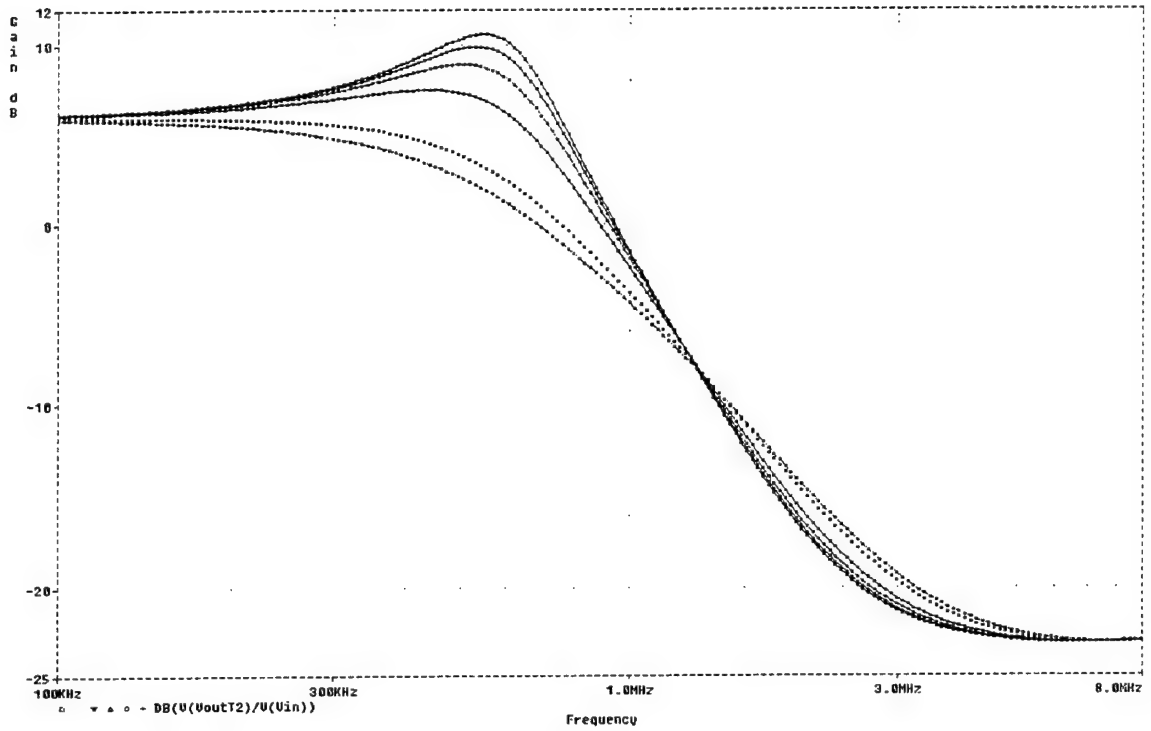
5. Low-Pass, Quality Factor = 4, All Frequencies



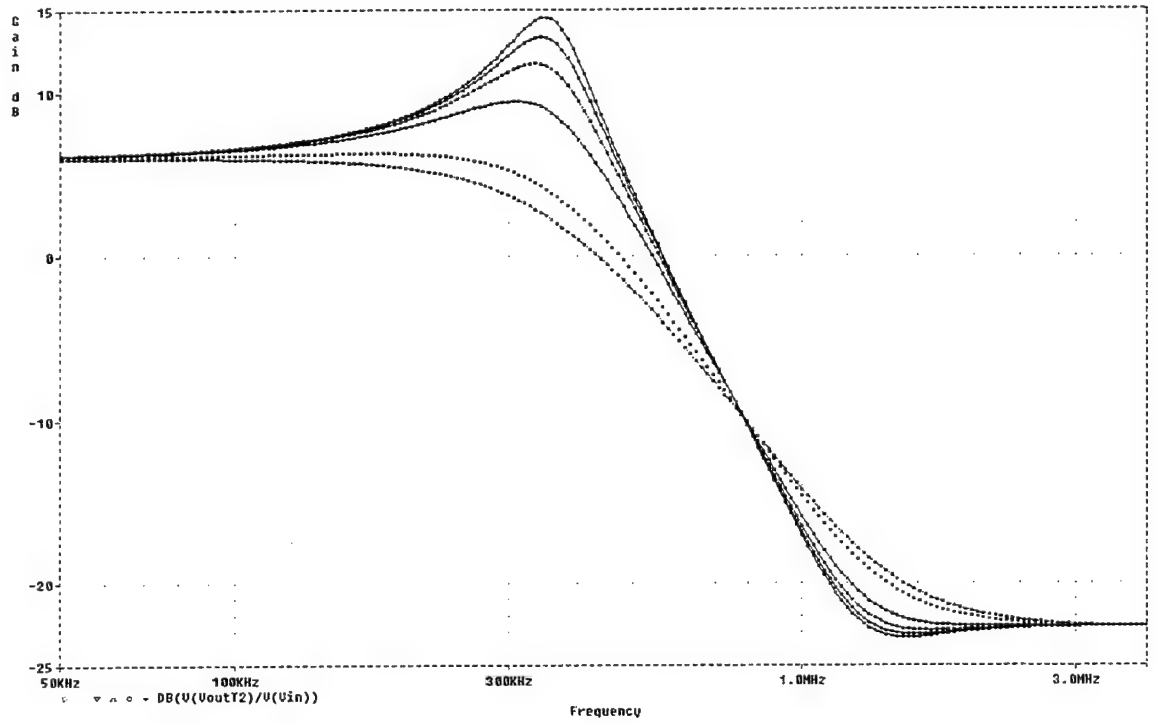
6. Low-Pass, Quality Factor = 5, All Frequencies



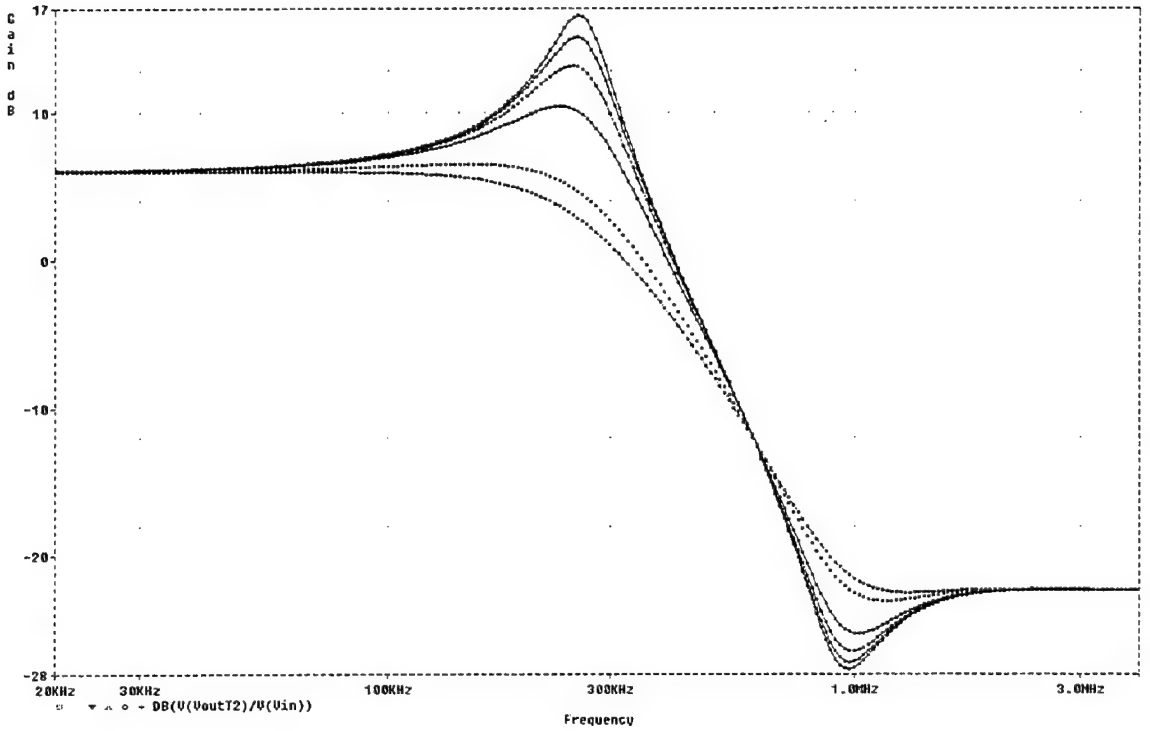
7. Low-Pass, Frequency = 994 kHz, All Quality Factors



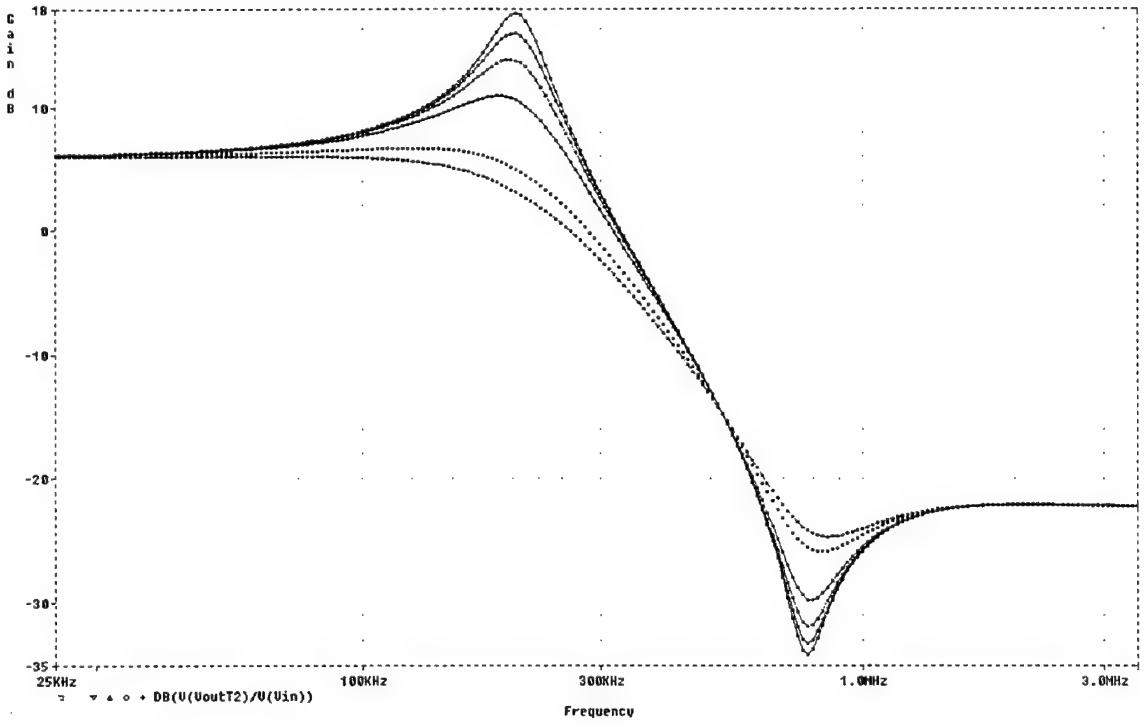
8. Low-Pass, Frequency = 497 kHz, All Quality Factors



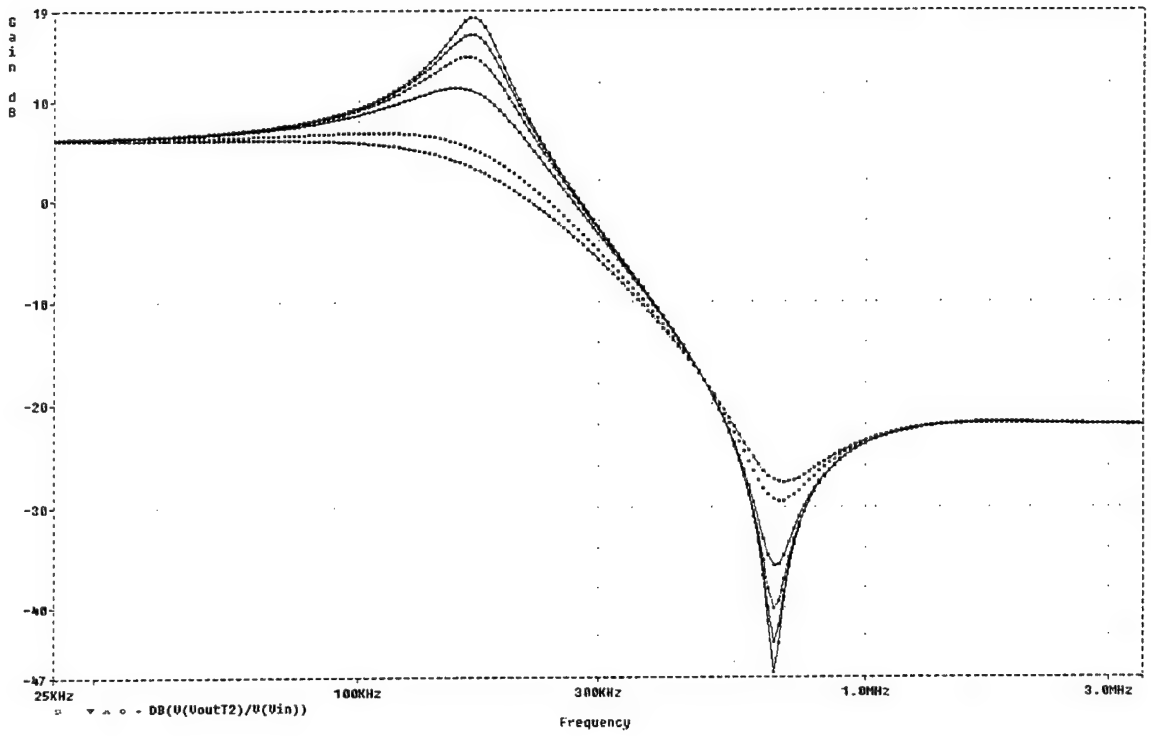
9. Low-Pass, Frequency = 331 kHz, All Quality Factors



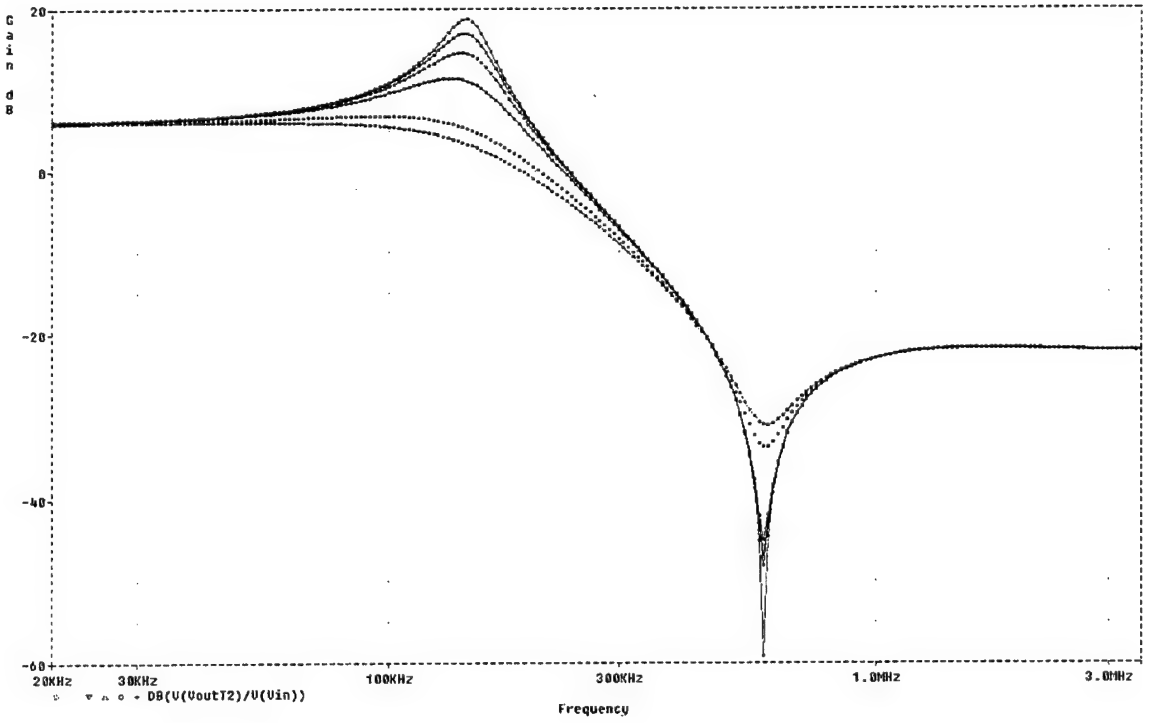
10. Low-Pass, Frequency = 249 kHz, All Quality Factors



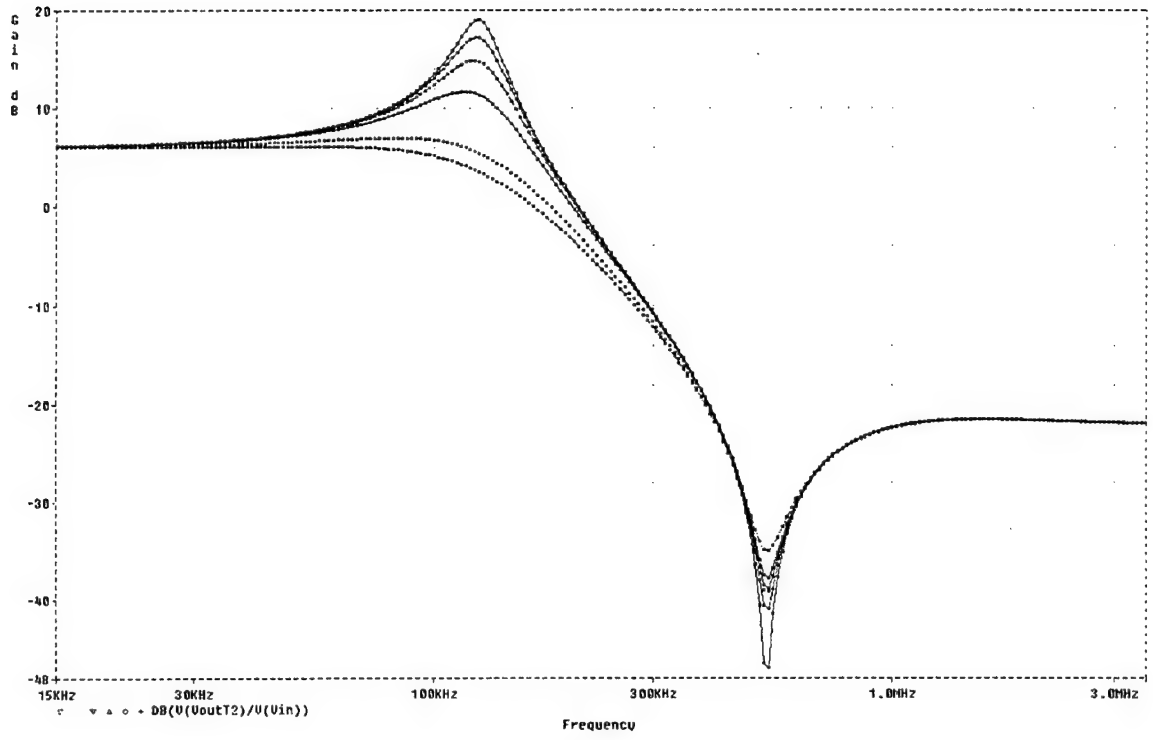
11. Low-Pass, Frequency = 199 kHz, All Quality Factors



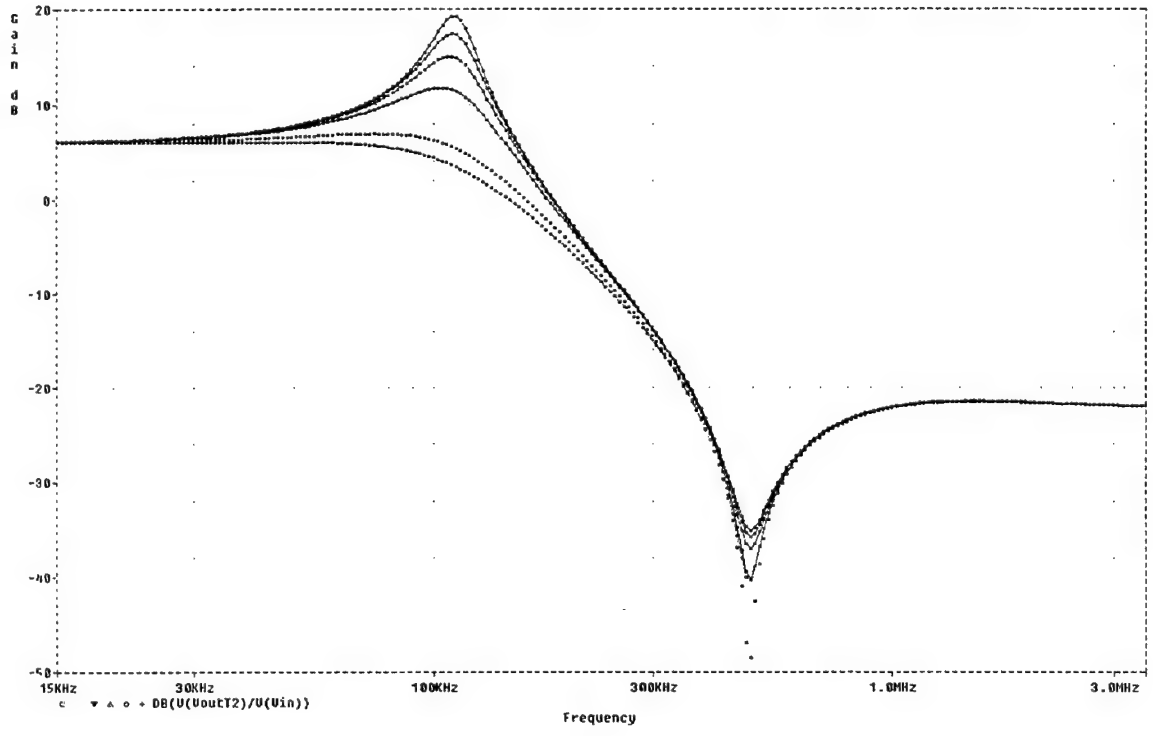
12. Low-Pass, Frequency = 166 kHz, All Quality Factors



13. Low-Pass, Frequency = 142 kHz, All Quality Factors

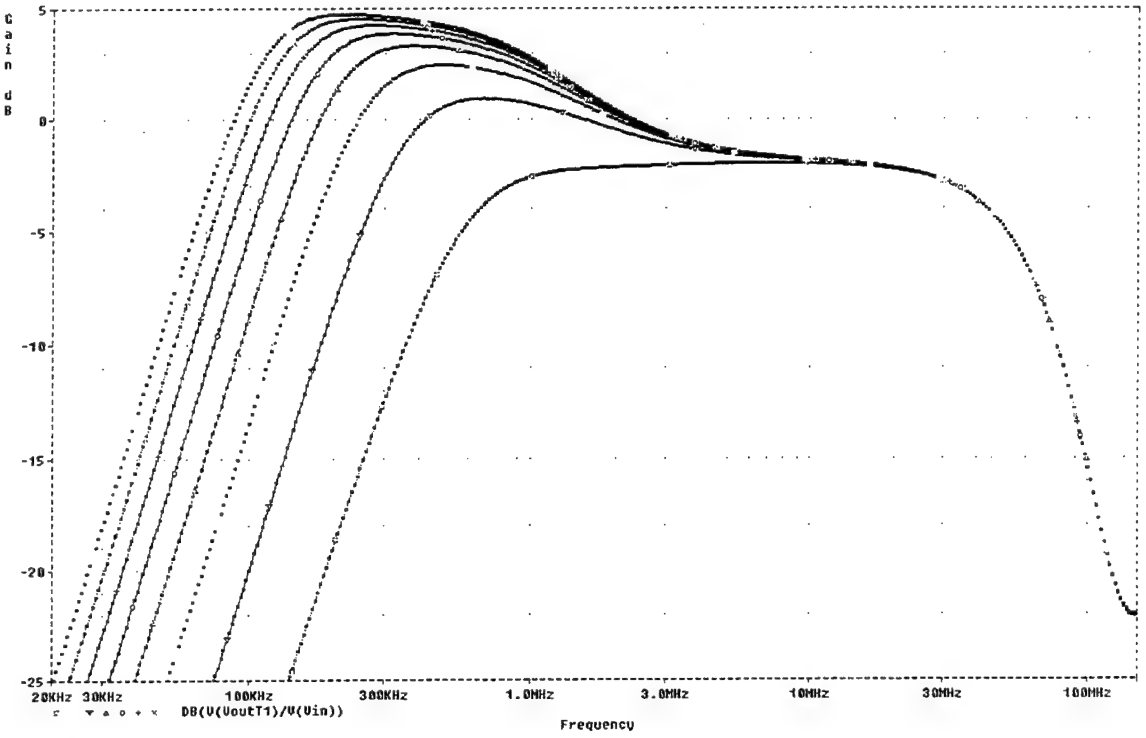


14. Low-Pass, Frequency = 124 kHz, All Quality Factors

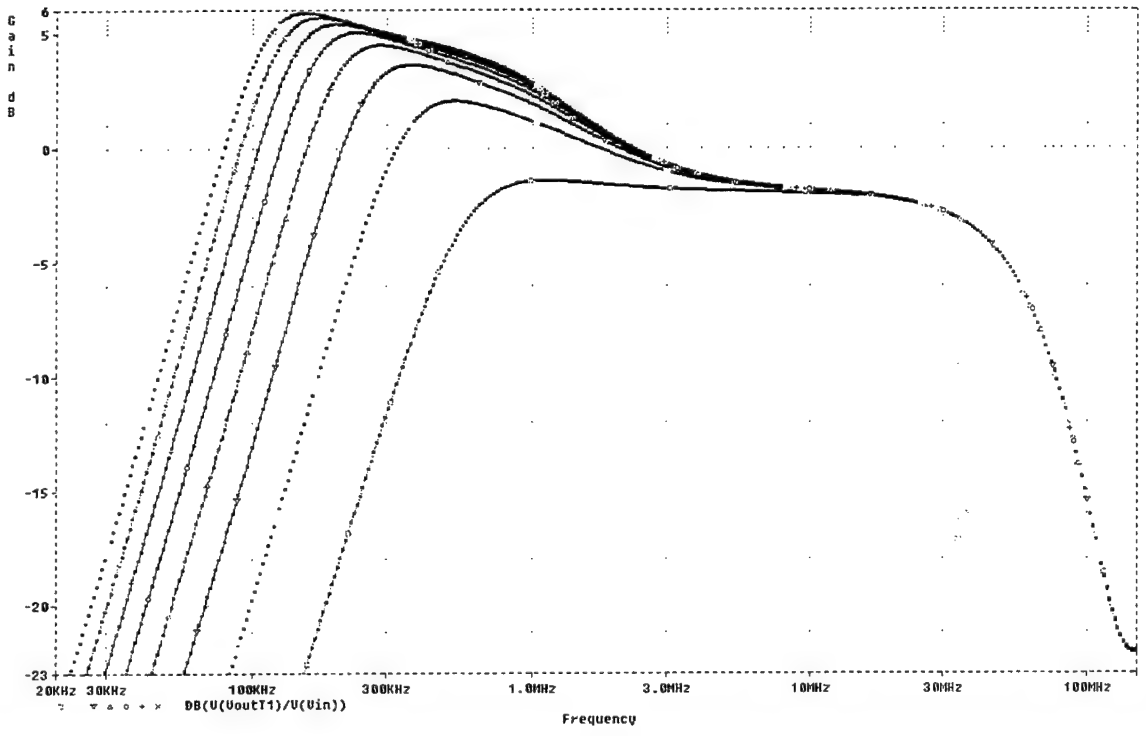


B. HIGH-PASS FILTER

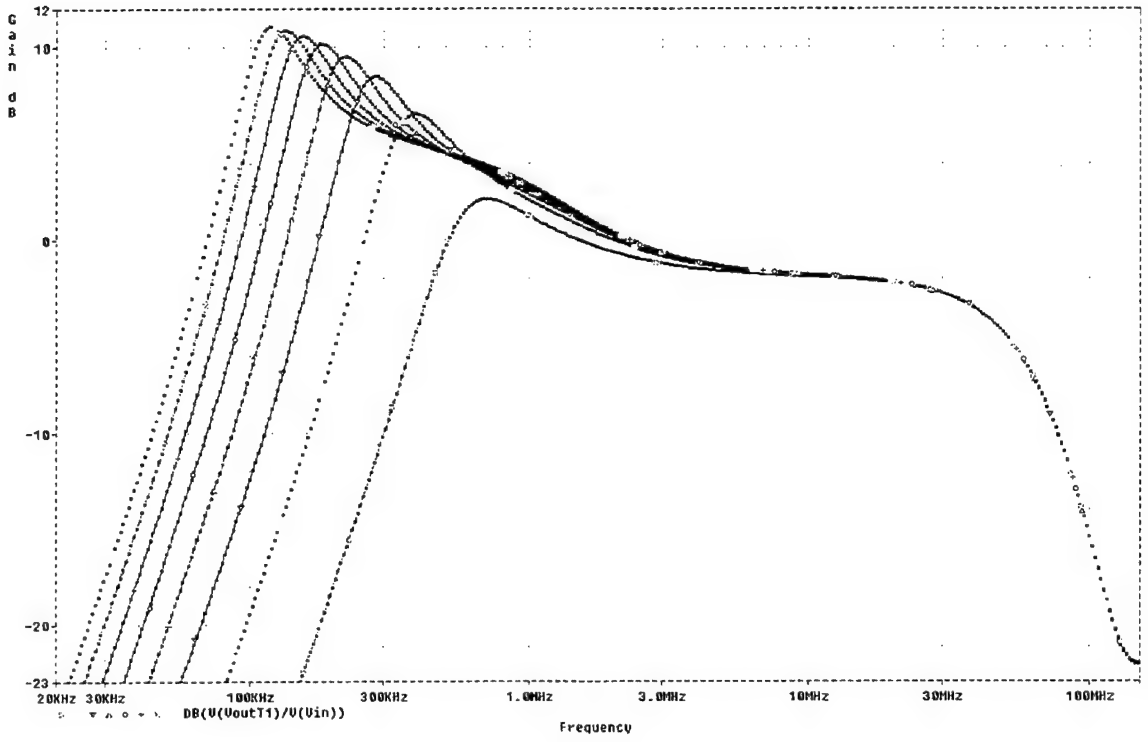
1. High-Pass, Quality Factor = 0.8, All Frequencies



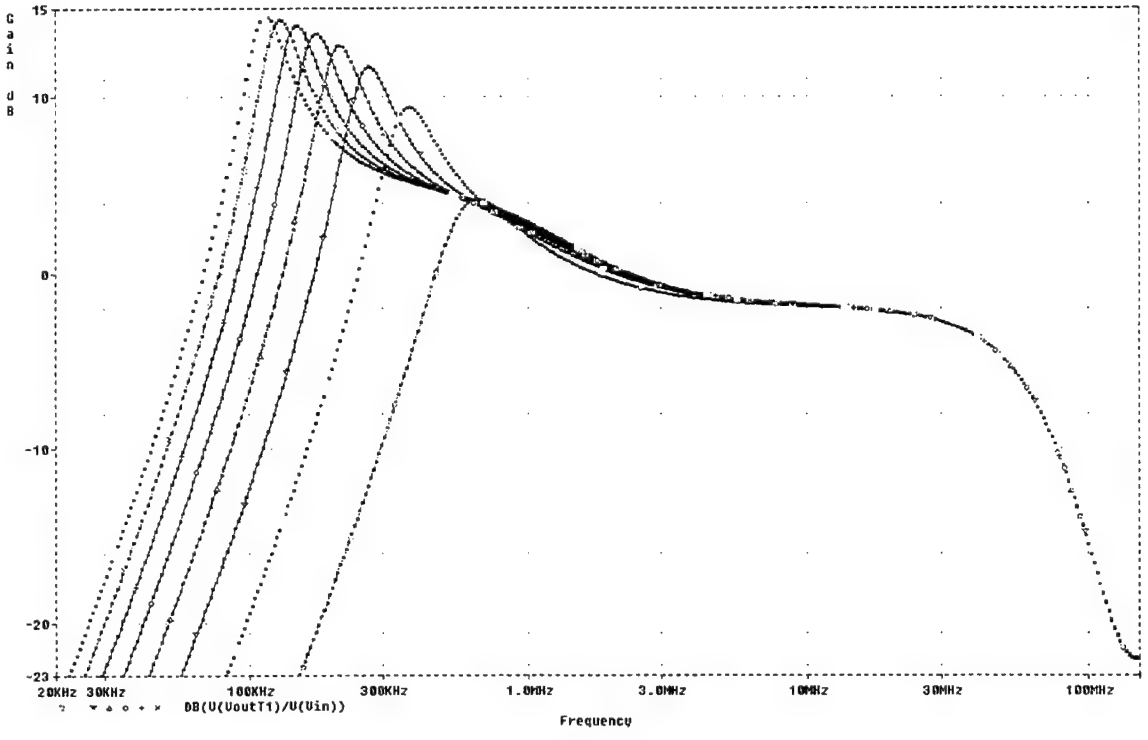
2. High-Pass, Quality Factor = 1, All Frequencies



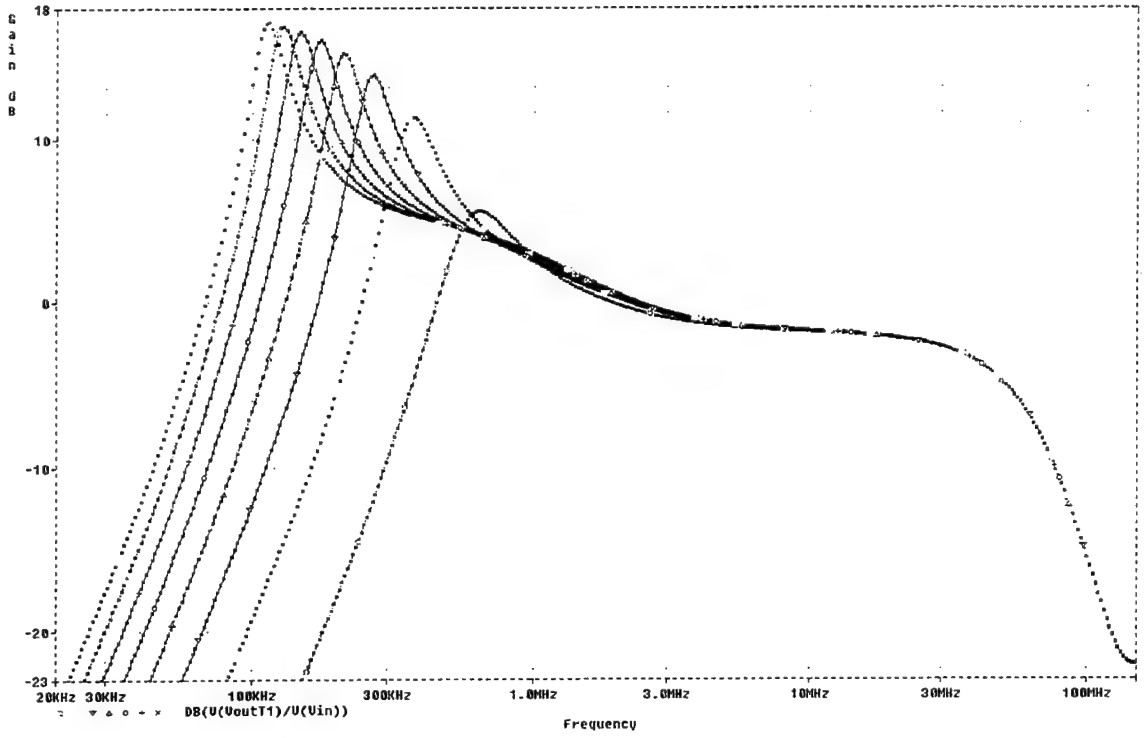
3. High-Pass, Quality Factor = 2, All Frequencies



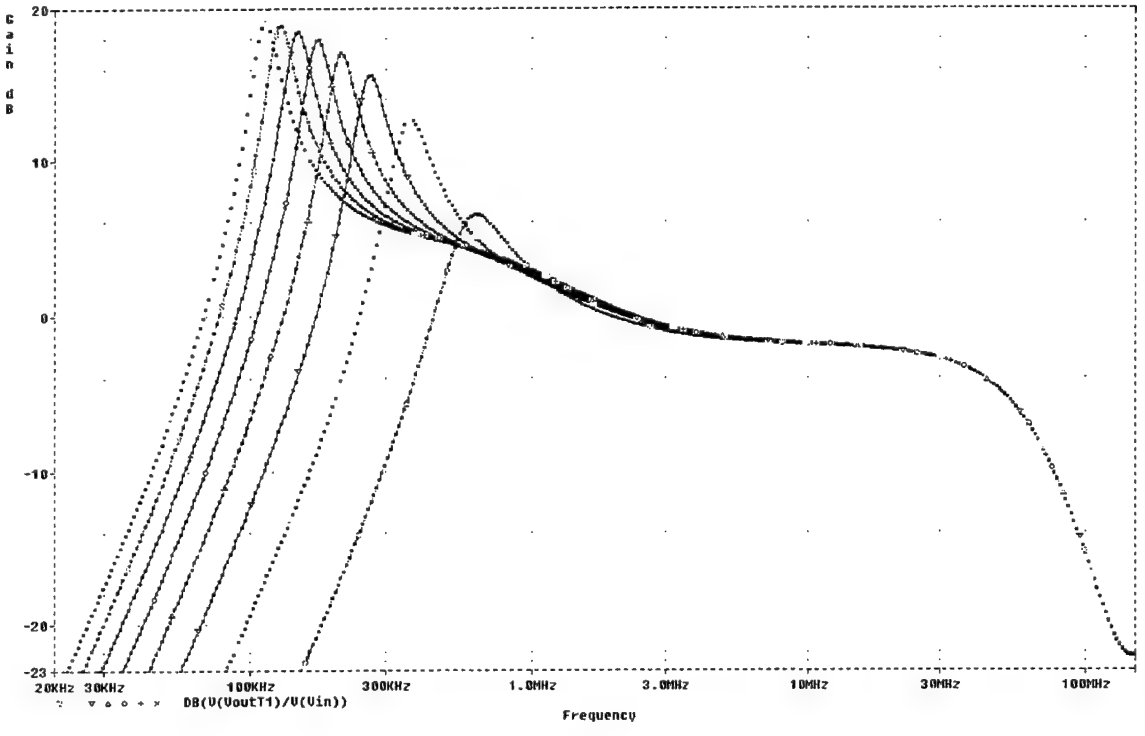
4. High-Pass, Quality Factor = 3, All Frequencies



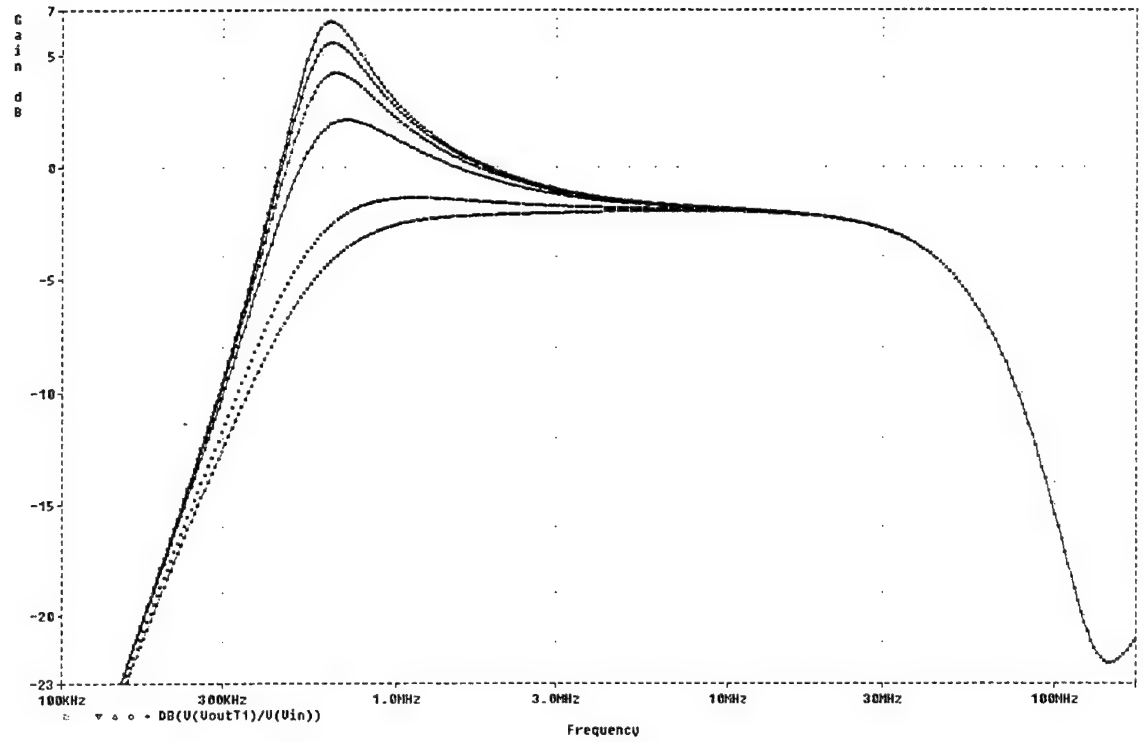
5. High-Pass, Quality Factor = 4, All Frequencies



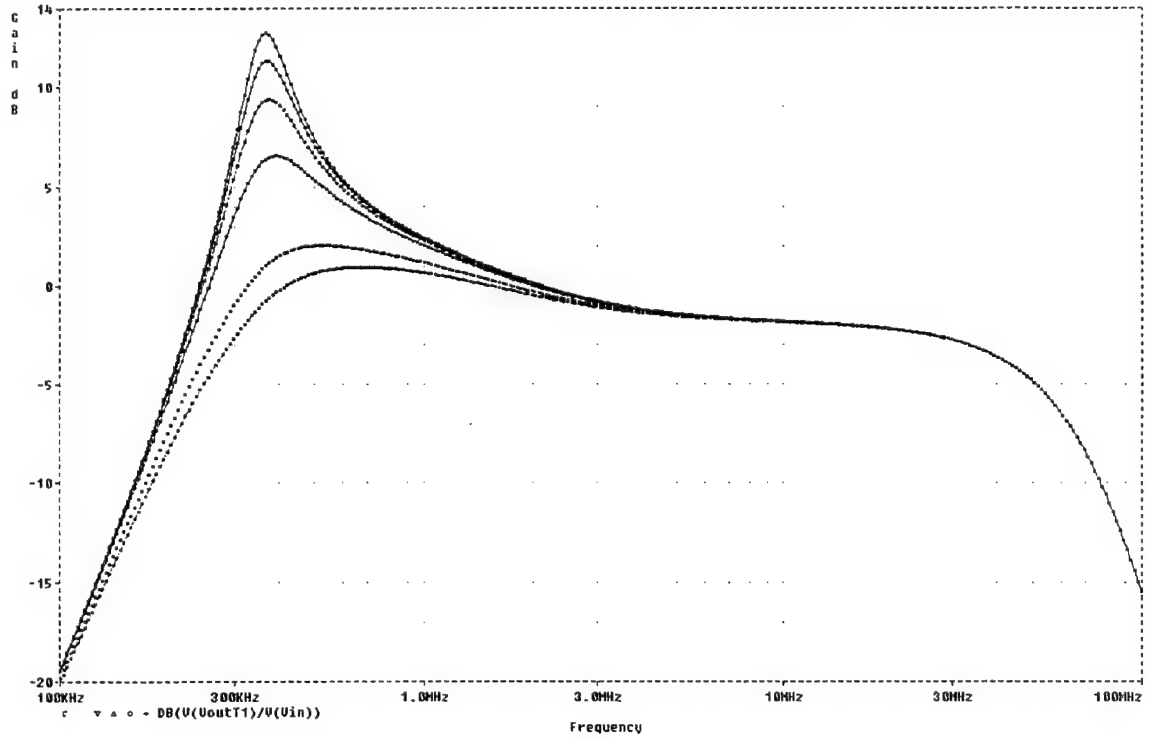
6. High-Pass, Quality Factor = 5, All Frequencies



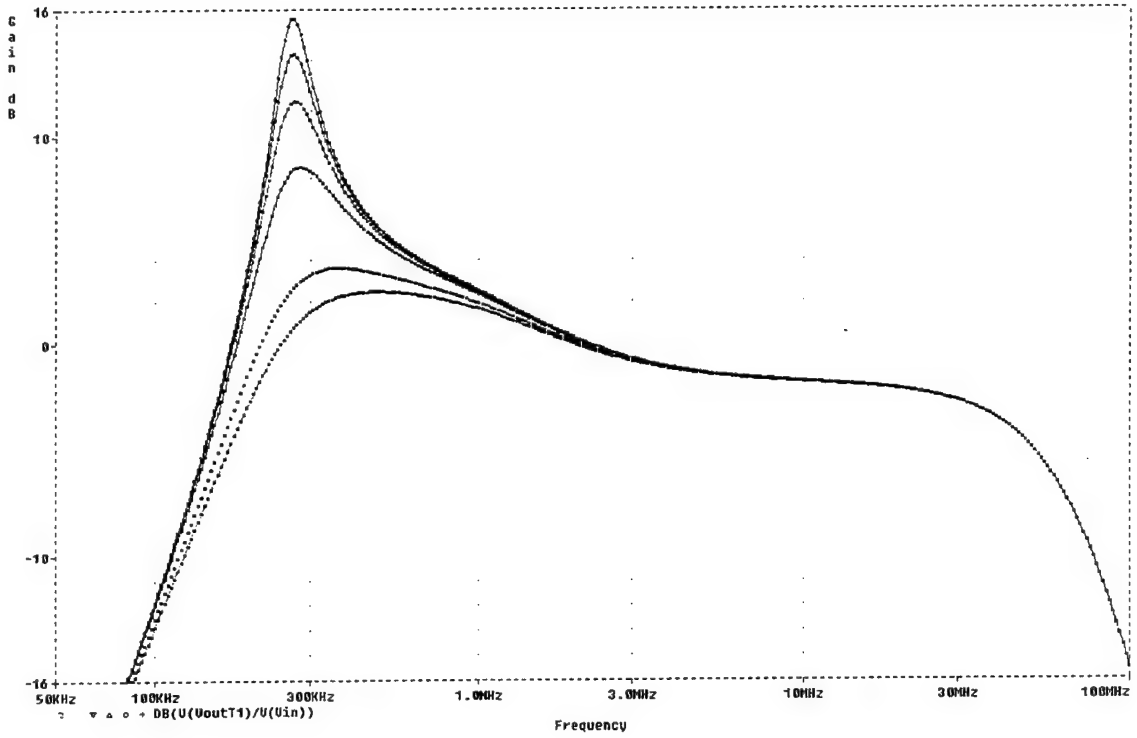
7. High-Pass, Frequency = 994 kHz, All Quality Factors



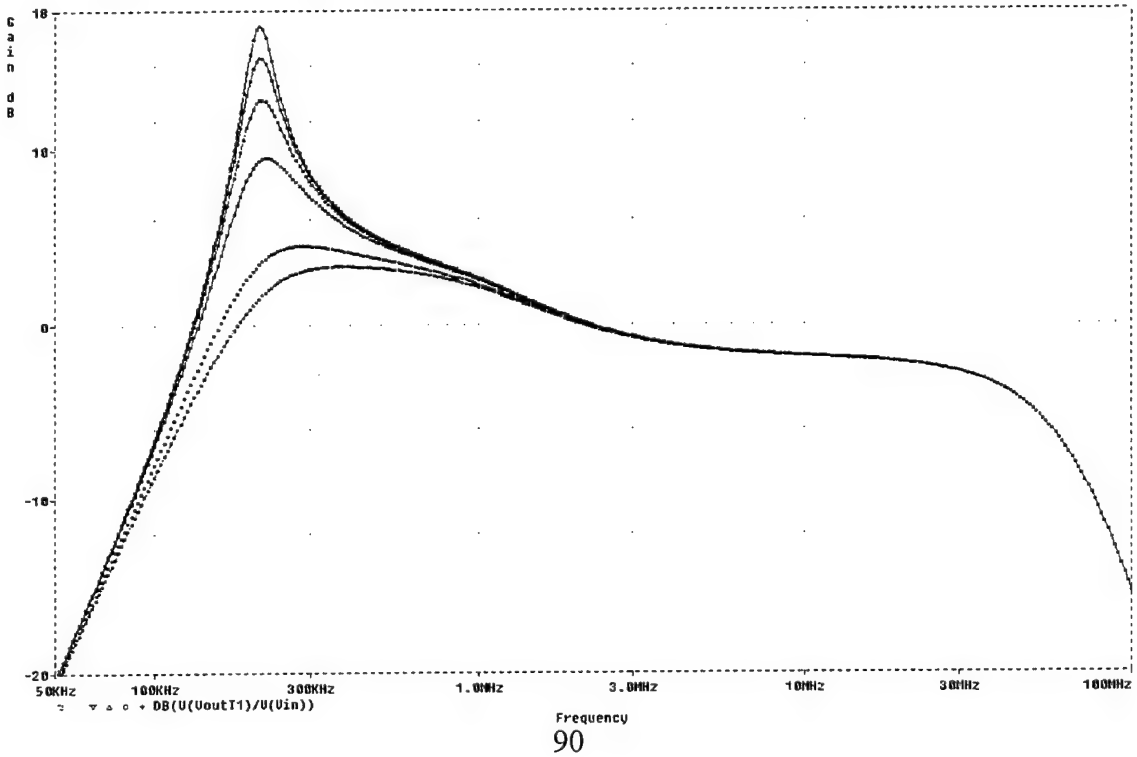
8. High-Pass, Frequency = 497 kHz, All Quality Factors



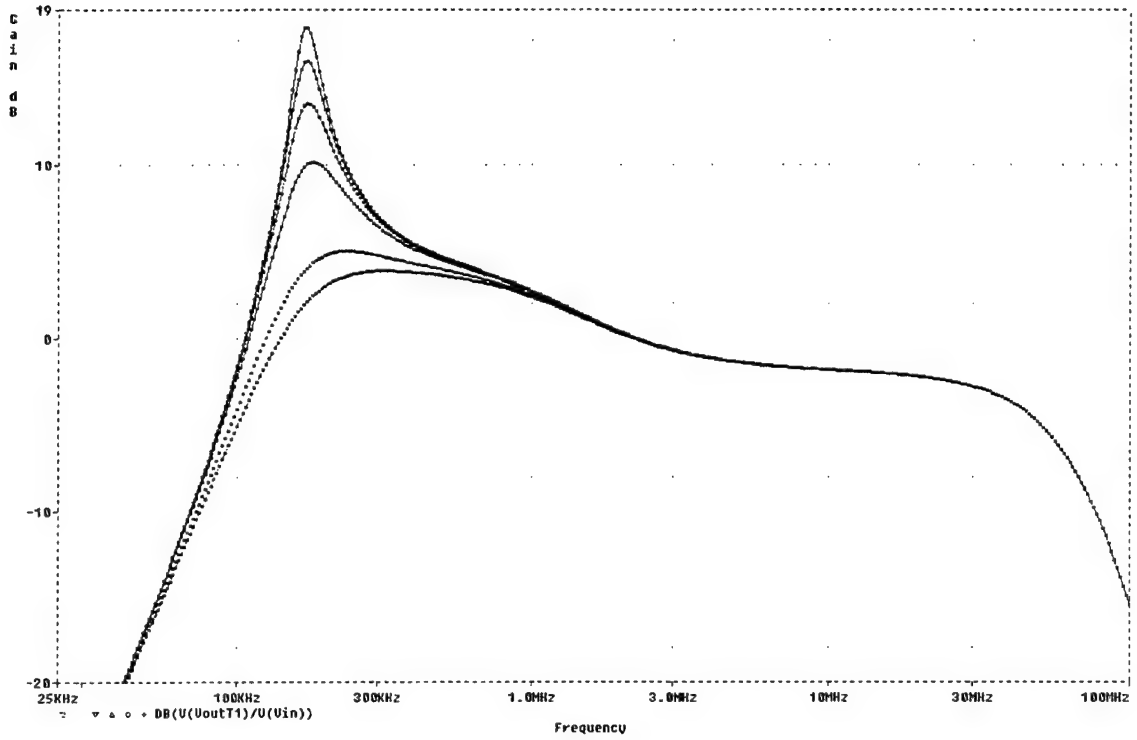
9. High-Pass, Frequency = 331 kHz, All Quality Factors



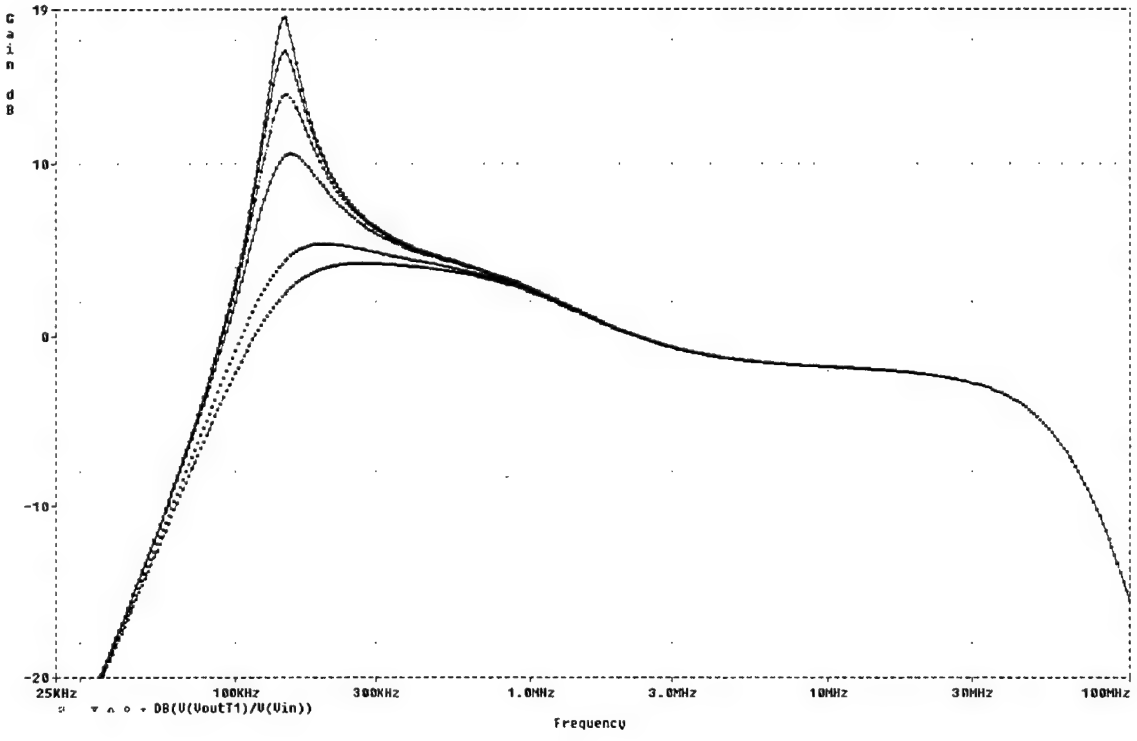
10. High-Pass, Frequency = 249 kHz, All Quality Factors



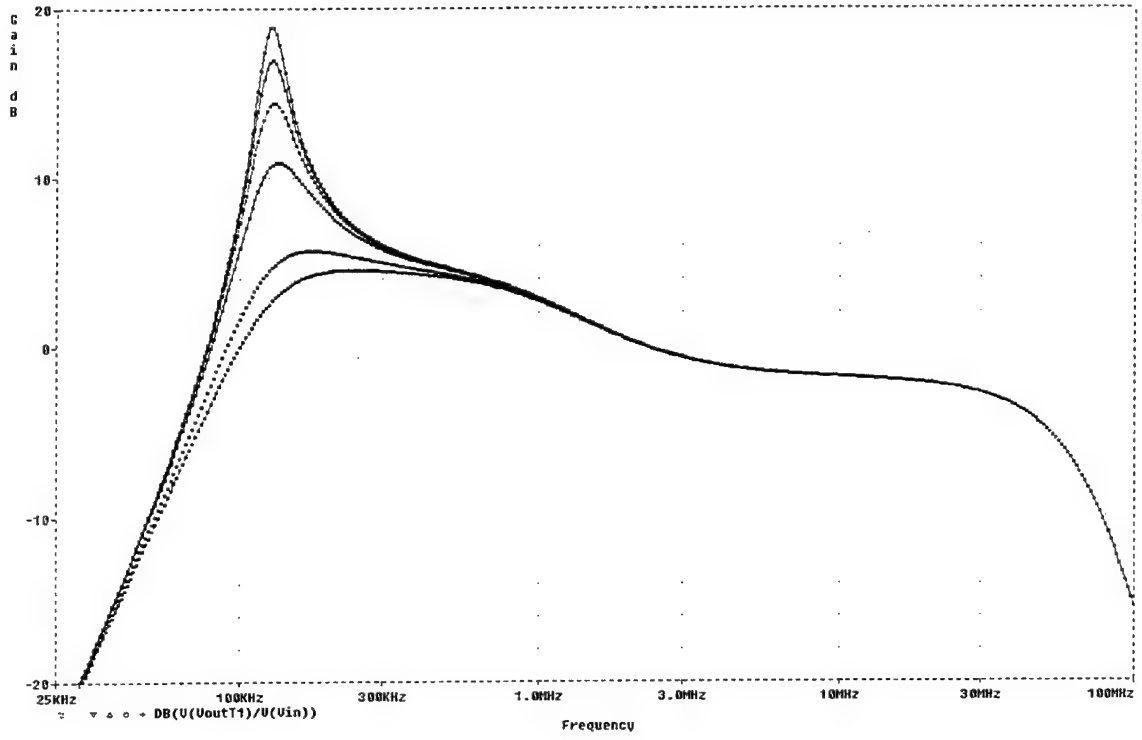
11. High-Pass, Frequency = 199 kHz, All Quality Factors



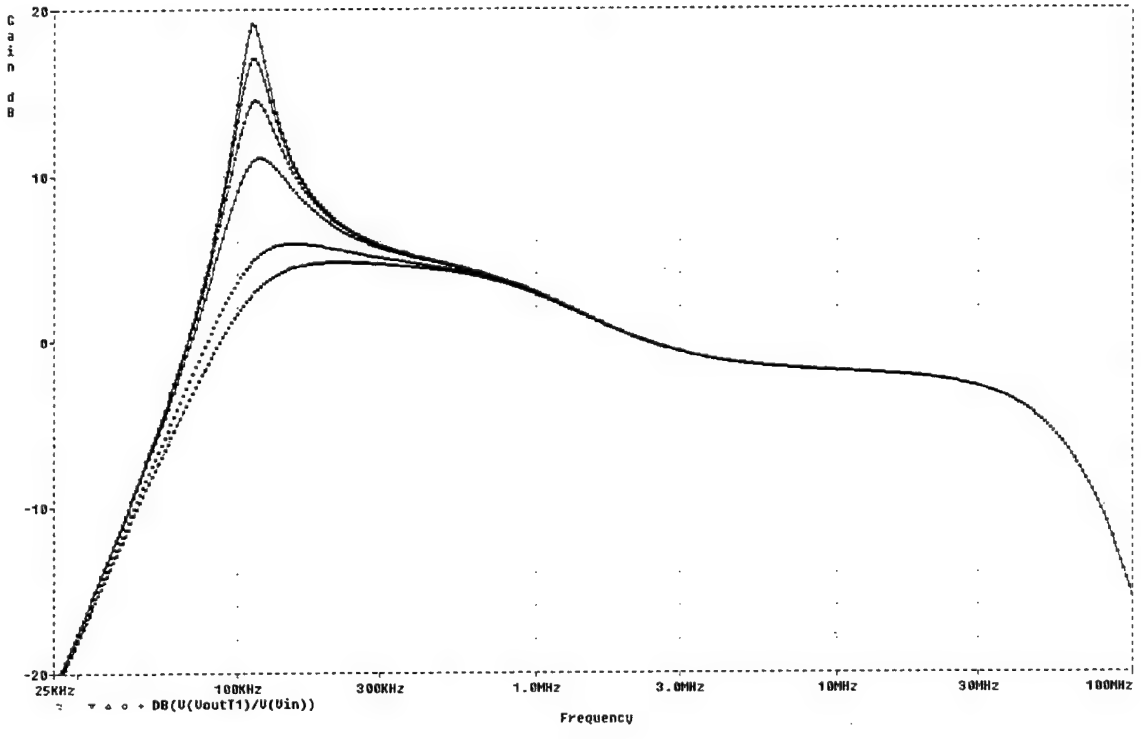
12. High-Pass, Frequency = 166 kHz, All Quality Factors



13. High-Pass, Frequency = 142 kHz, All Quality Factors

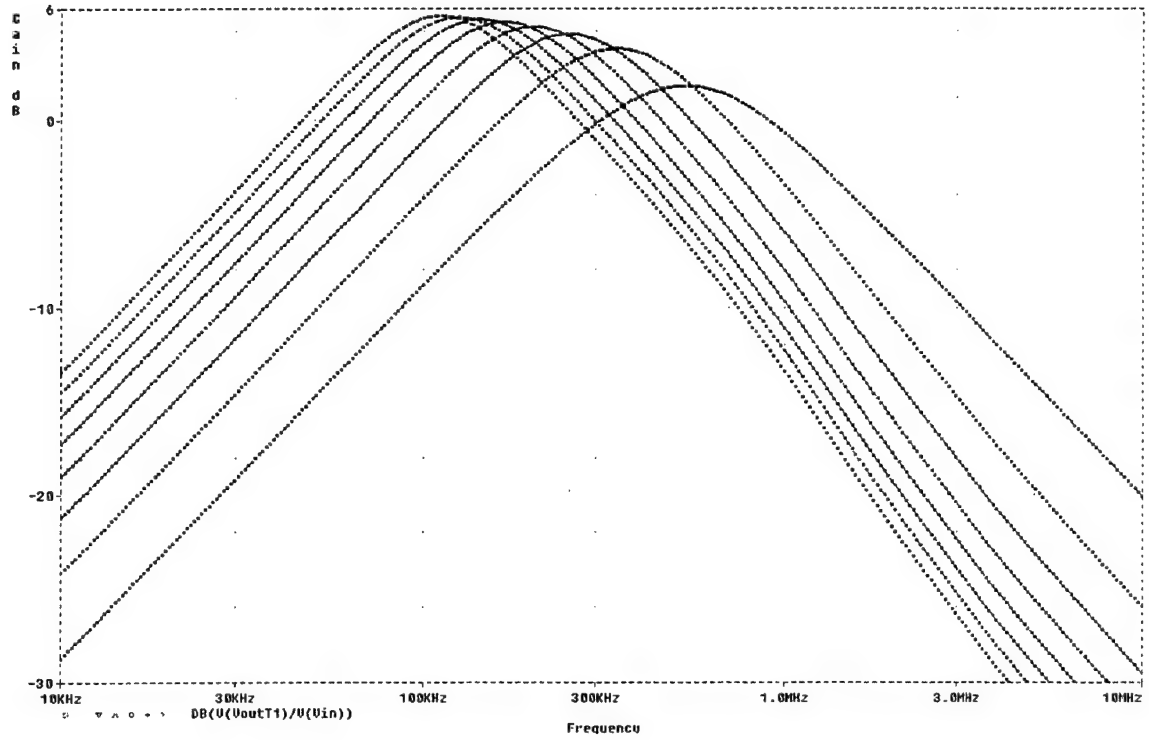


14. High-Pass, Frequency = 124 kHz, All Quality Factors

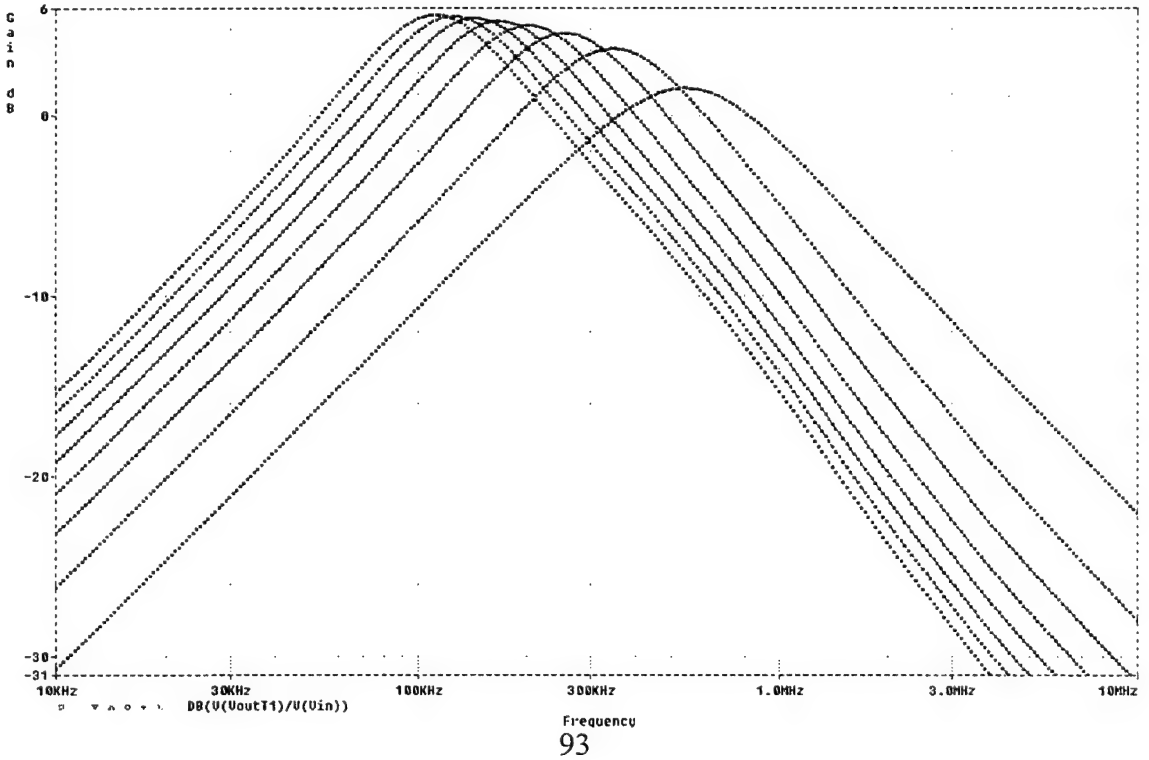


C. BAND-PASS FILTER

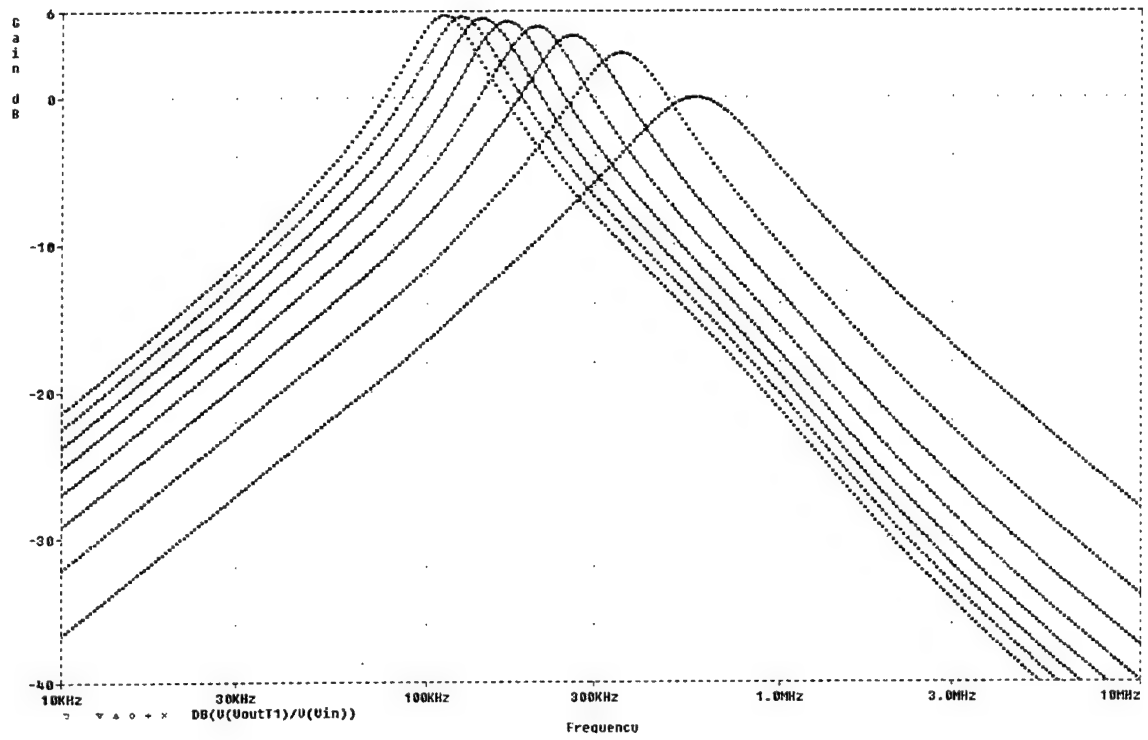
1. Band-Pass, Quality Factor = 0.8, All Frequencies



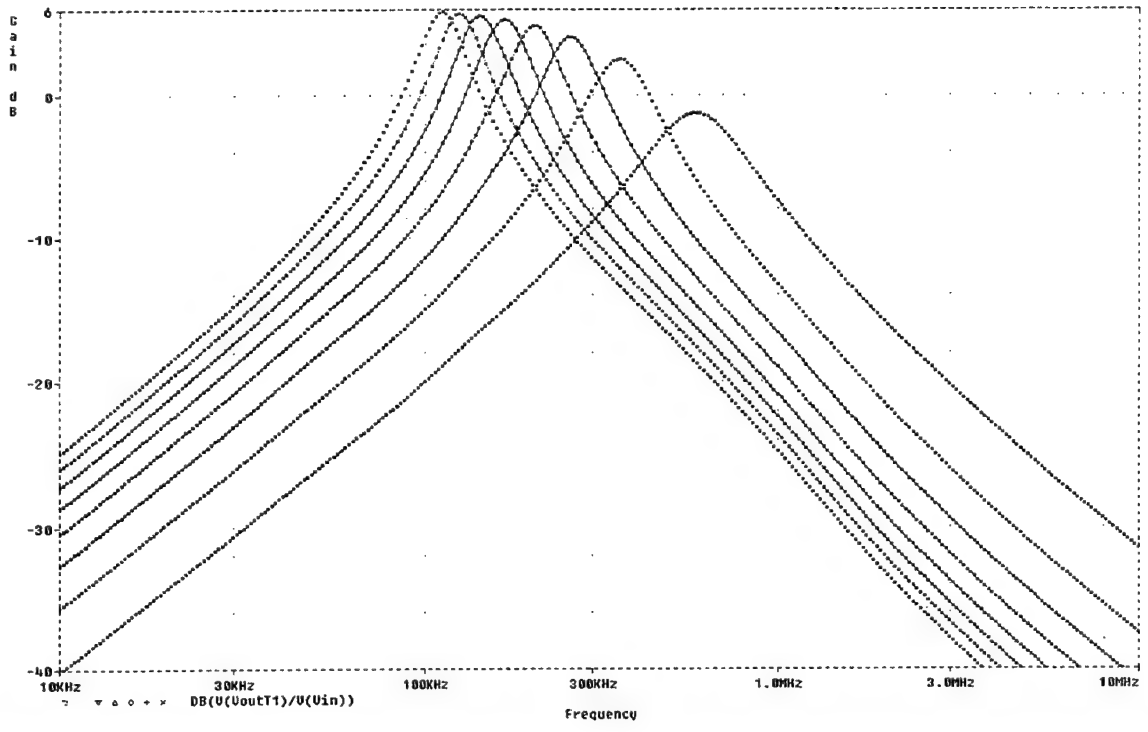
2. Band-Pass, Quality Factor = 1, All Frequencies



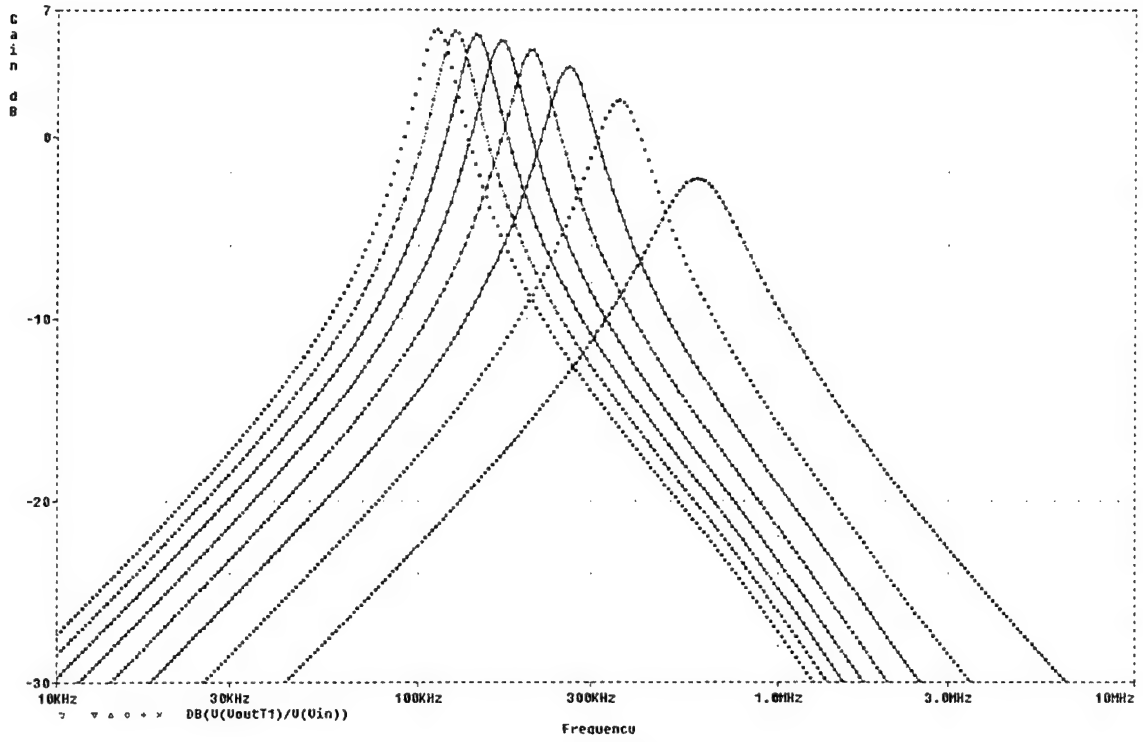
3. Band-Pass, Quality Factor = 2, All Frequencies



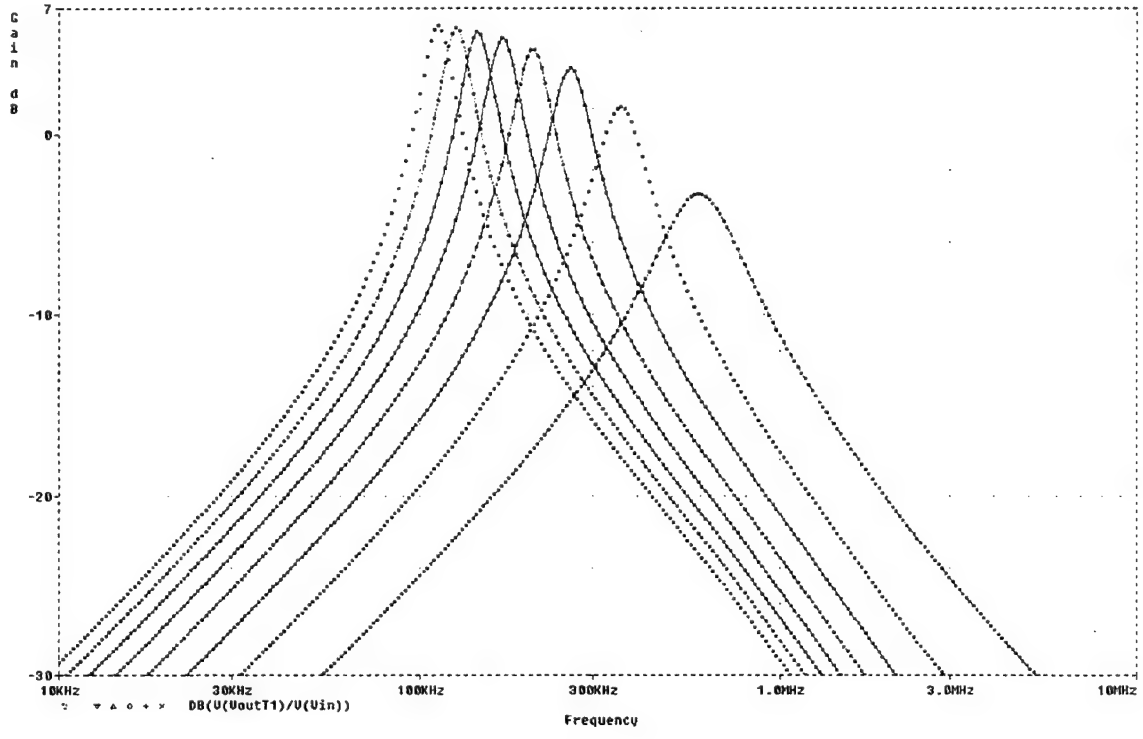
4. Band-Pass, Quality Factor = 3, All Frequencies



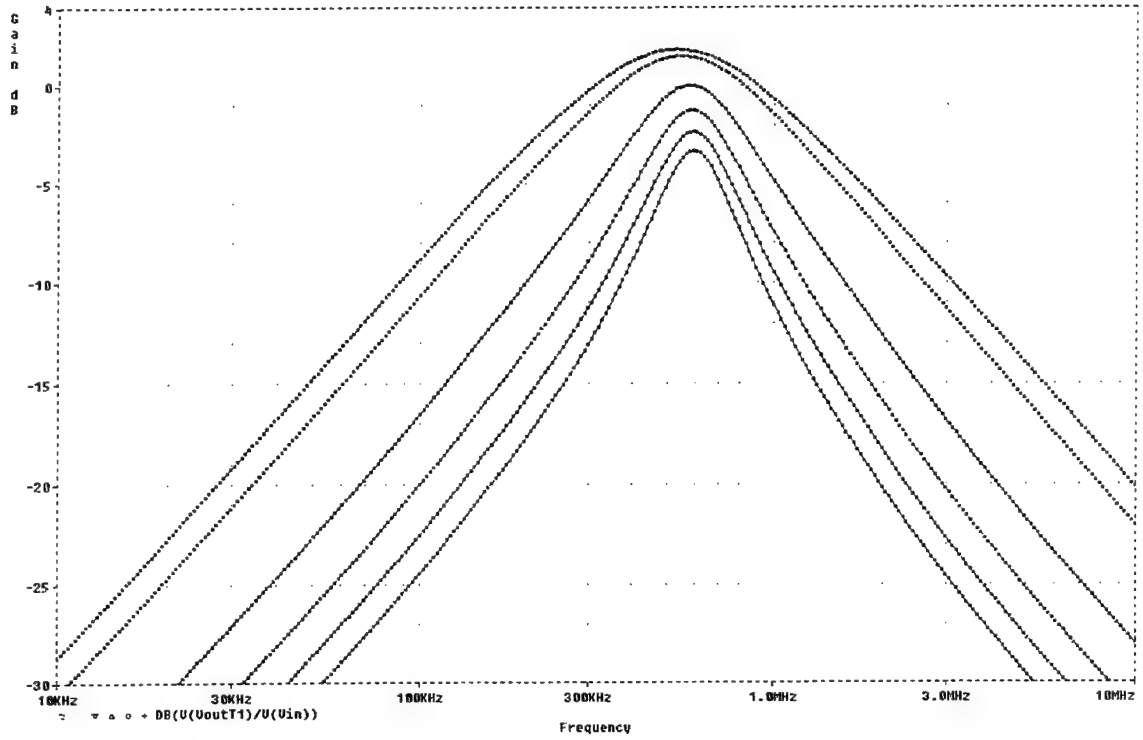
5. Band-Pass, Quality Factor = 4, All Frequencies



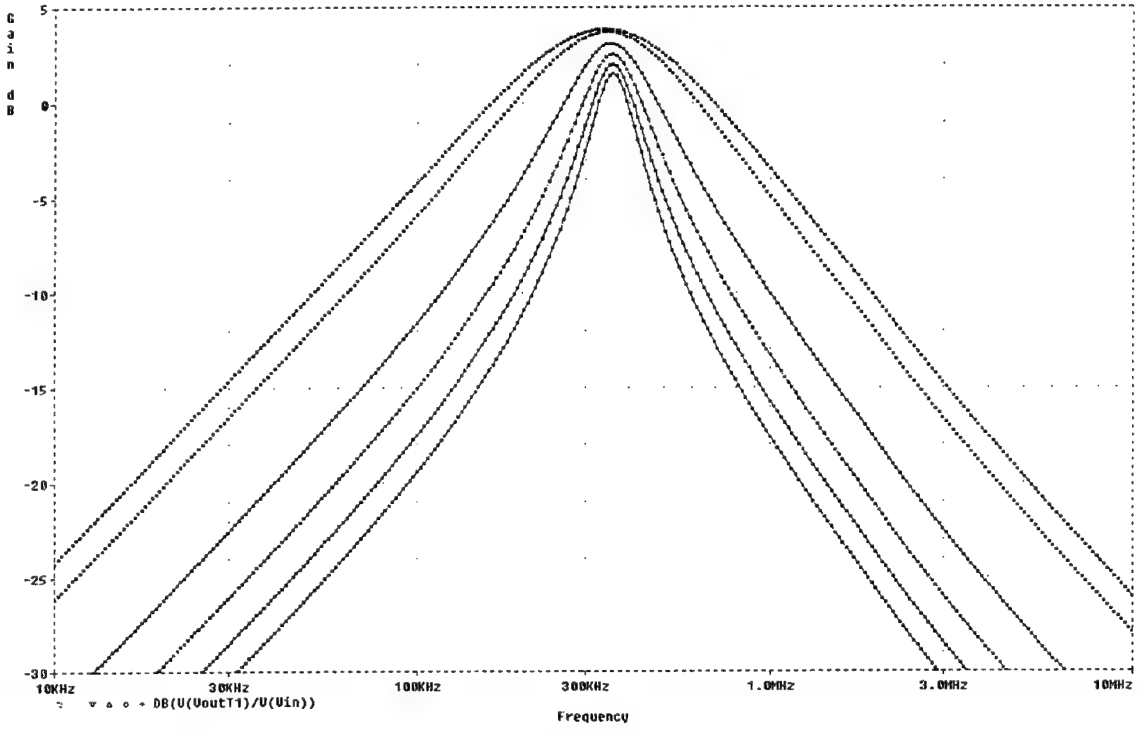
6. Band-Pass, Quality Factor = 5, All Frequencies



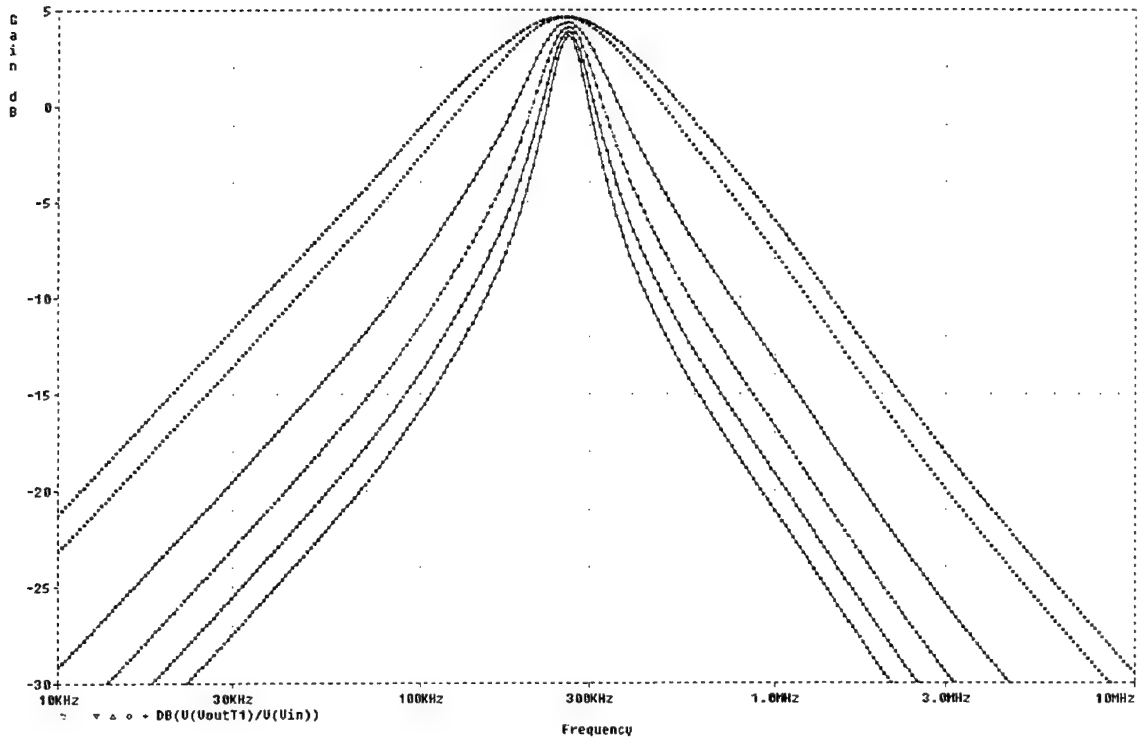
7. Band-Pass, Frequency = 994 kHz, All Quality Factors



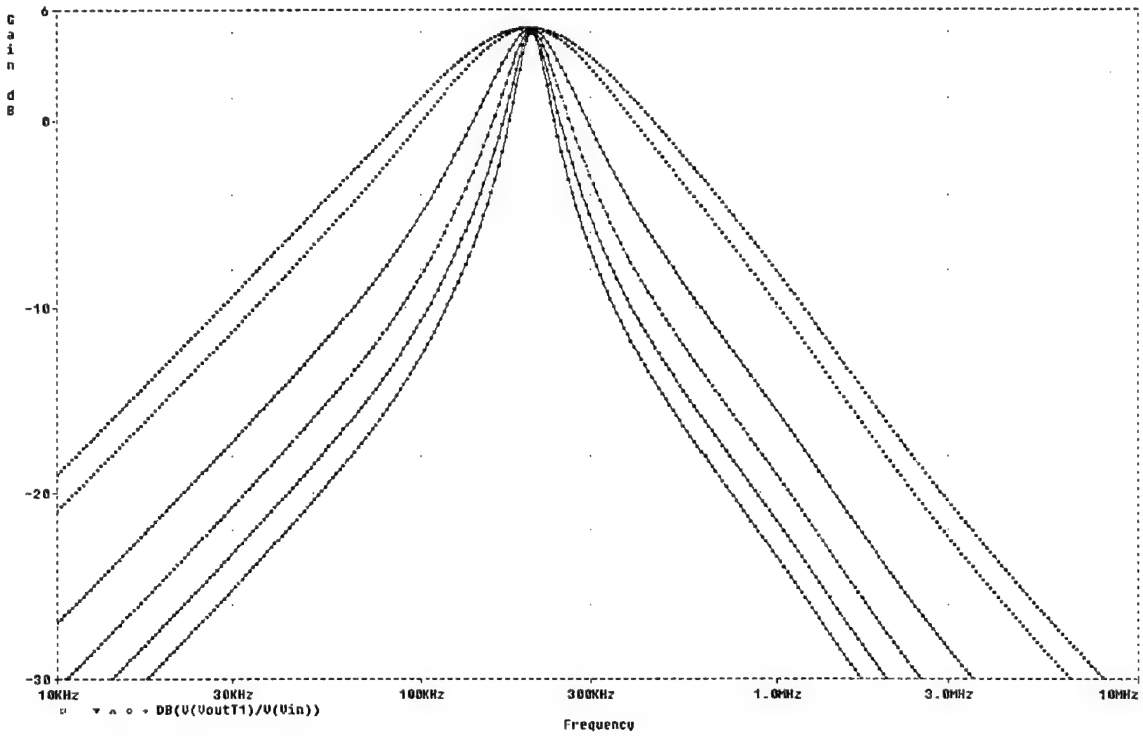
8. Band-Pass, Frequency = 497 kHz, All Quality Factors



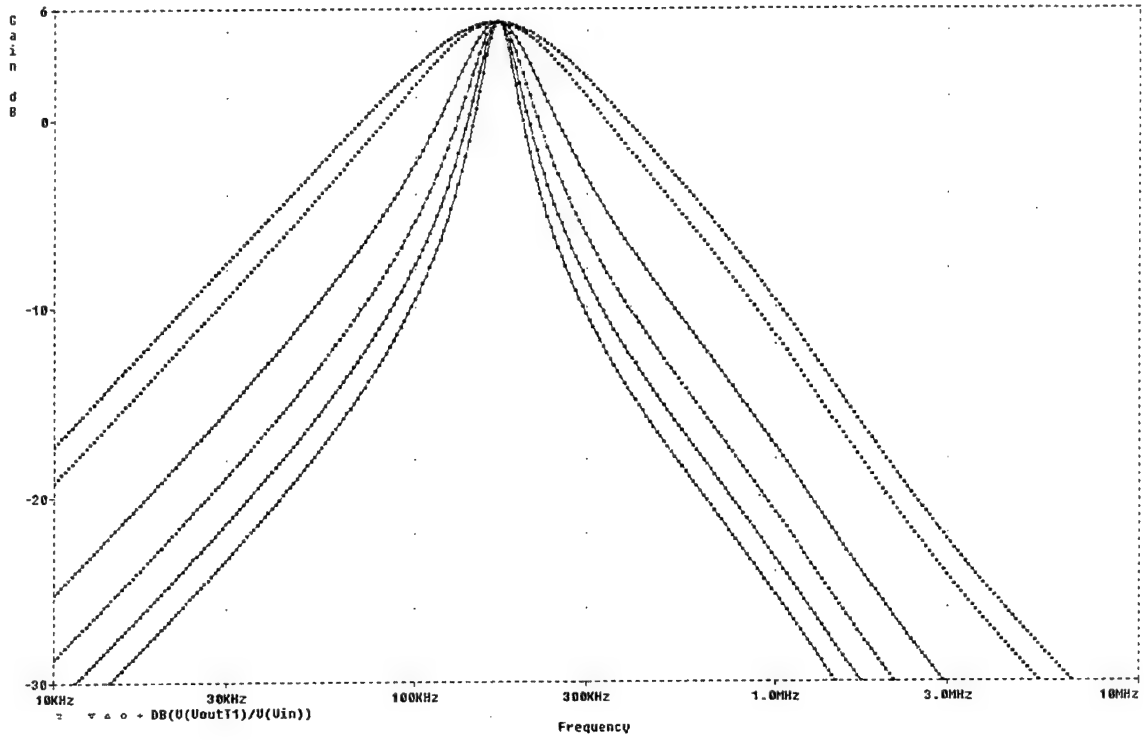
9. Band-Pass, Frequency = 331 kHz, All Quality Factors



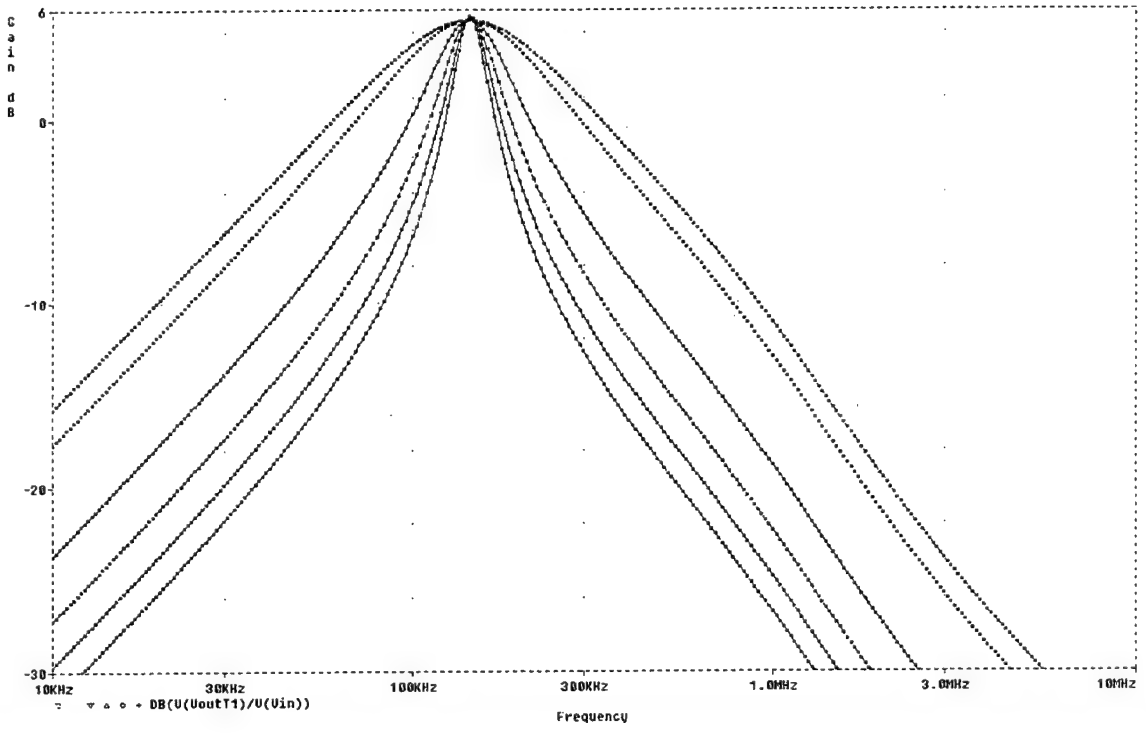
10. Band-Pass, Frequency = 249 kHz, All Quality Factors



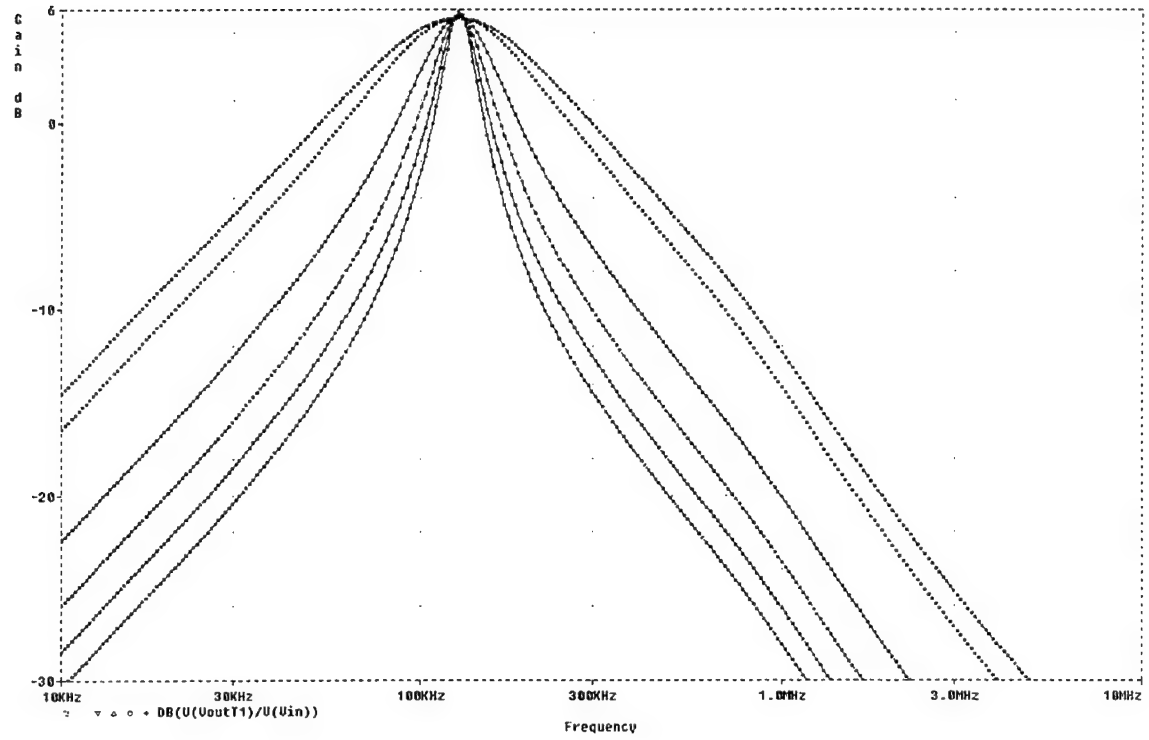
11. Band-Pass, Frequency = 199 kHz, All Quality Factors



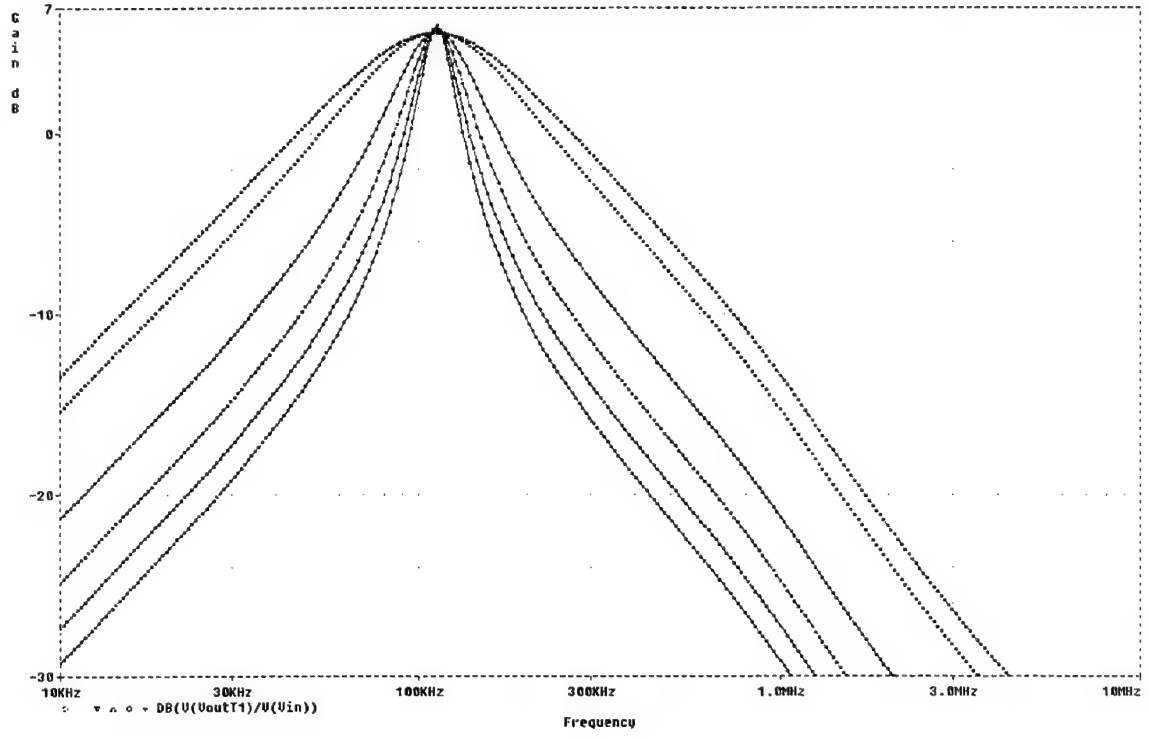
12. Band-Pass, Frequency = 166 kHz, All Quality Factors



13. Band-Pass, Frequency = 142 kHz, All Quality Factors

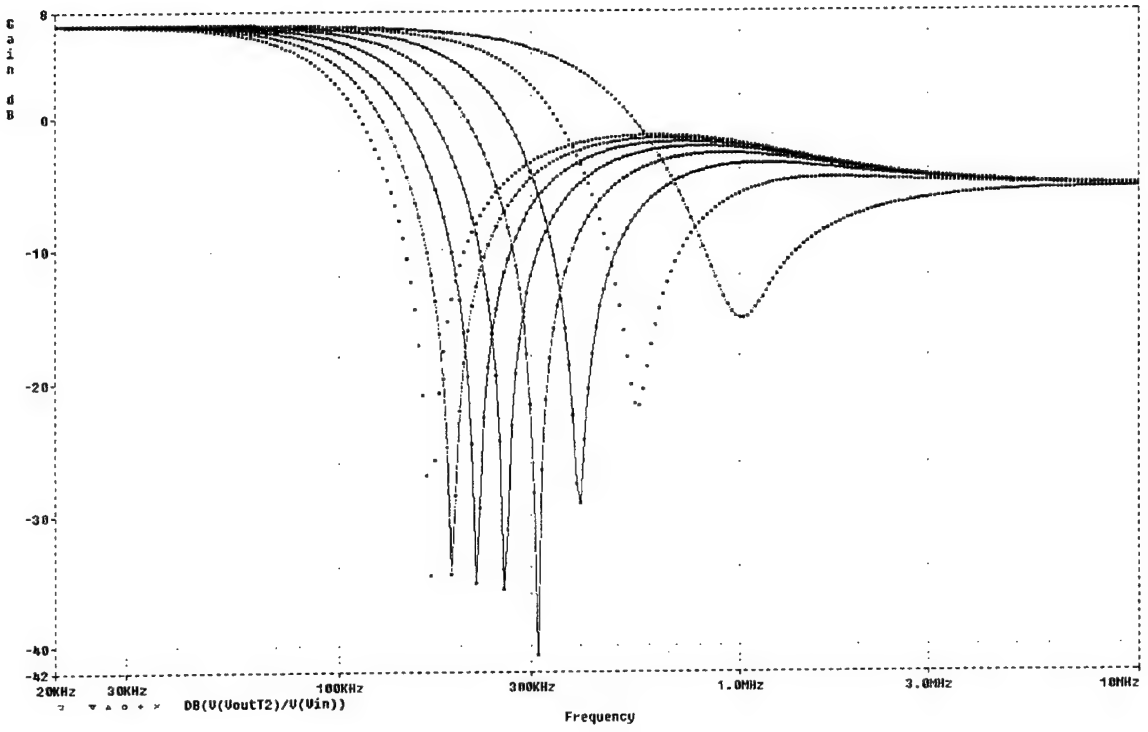


14. Band-Pass, Frequency = 124 kHz, All Quality Factors

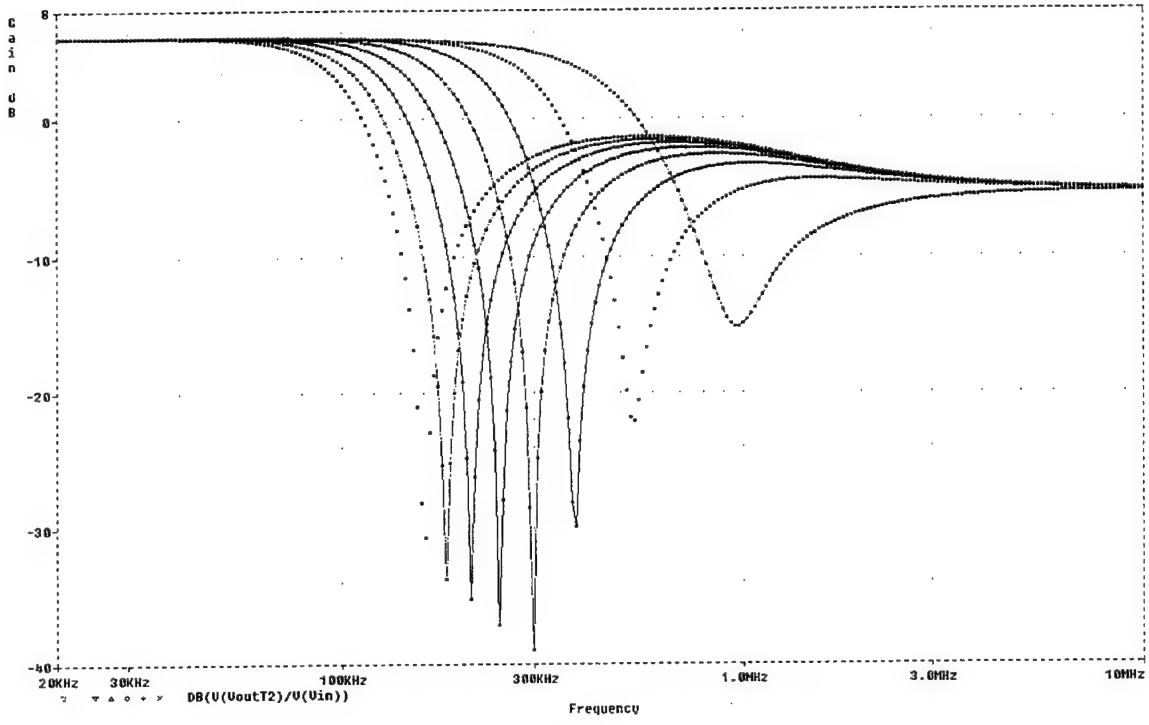


D. NOTCH FILTER

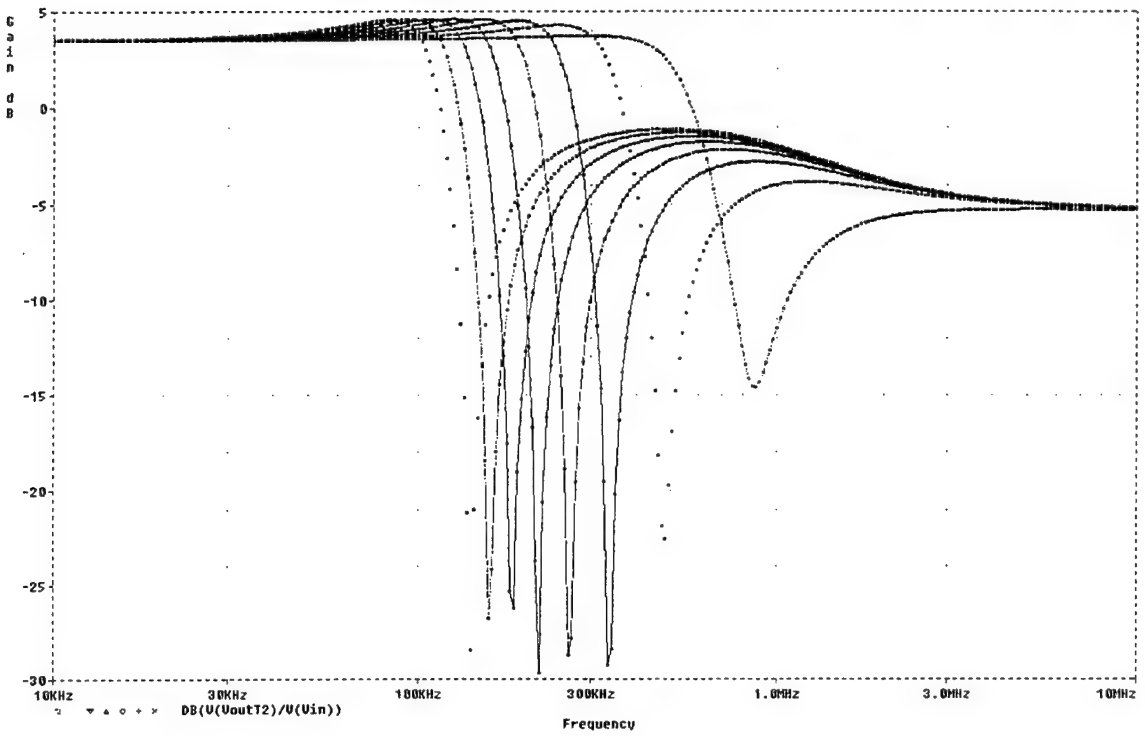
1. Notch, Quality Factor = 0.8, All Frequencies



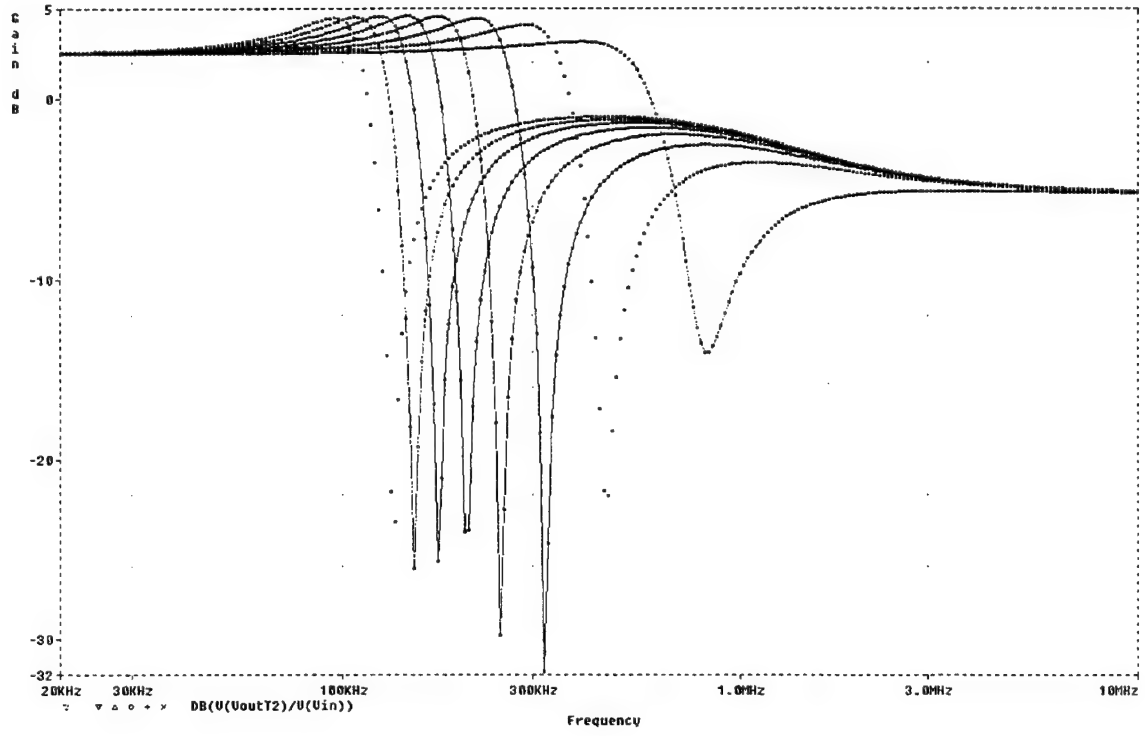
2. Notch, Quality Factor = 1, All Frequencies



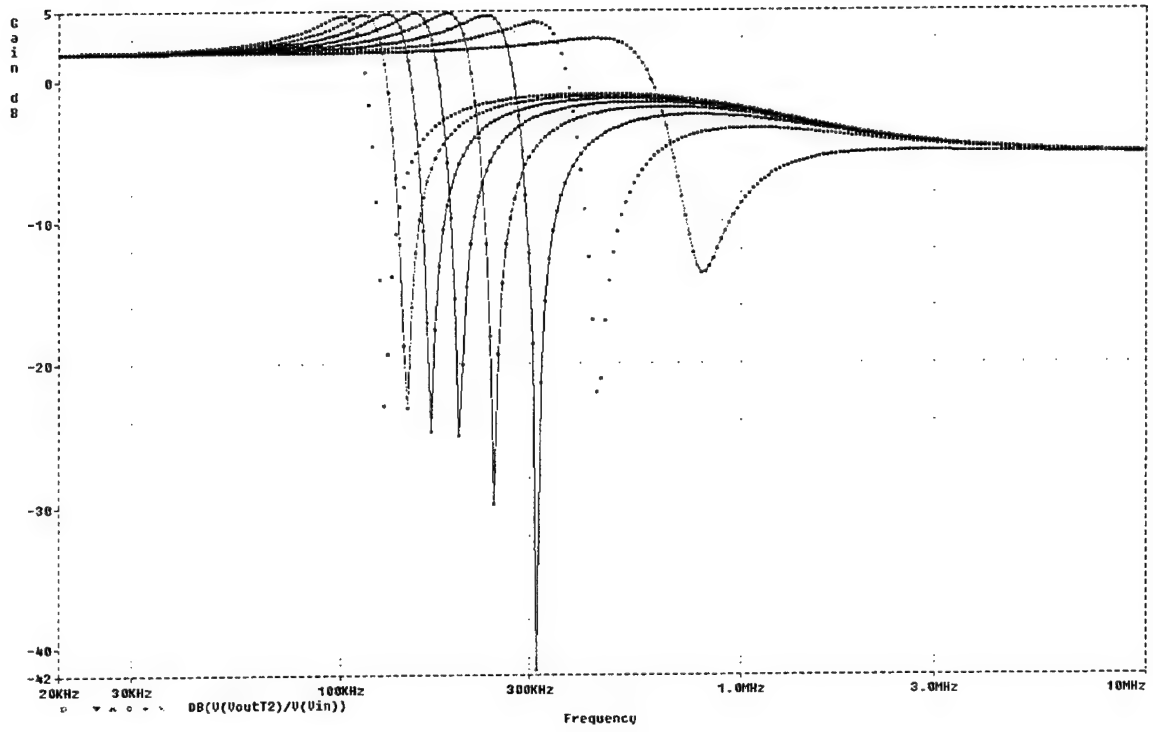
3. Notch, Quality Factor = 2, All Frequencies



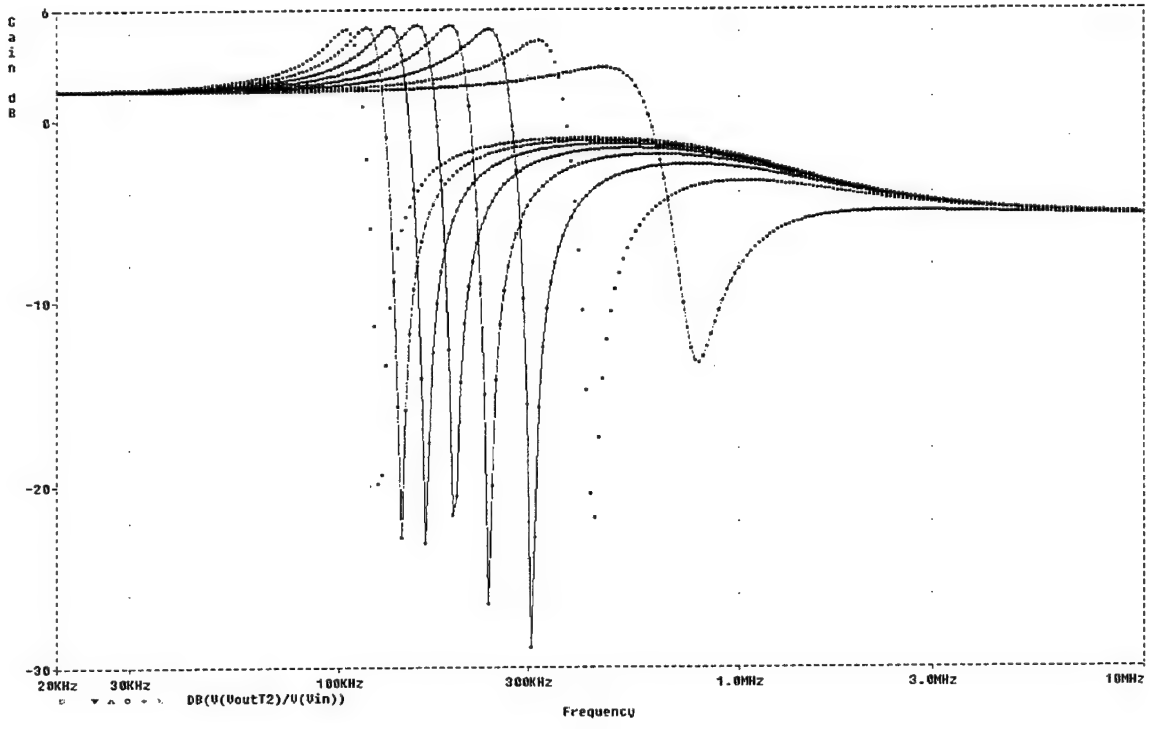
4. Notch, Quality Factor = 3, All Frequencies



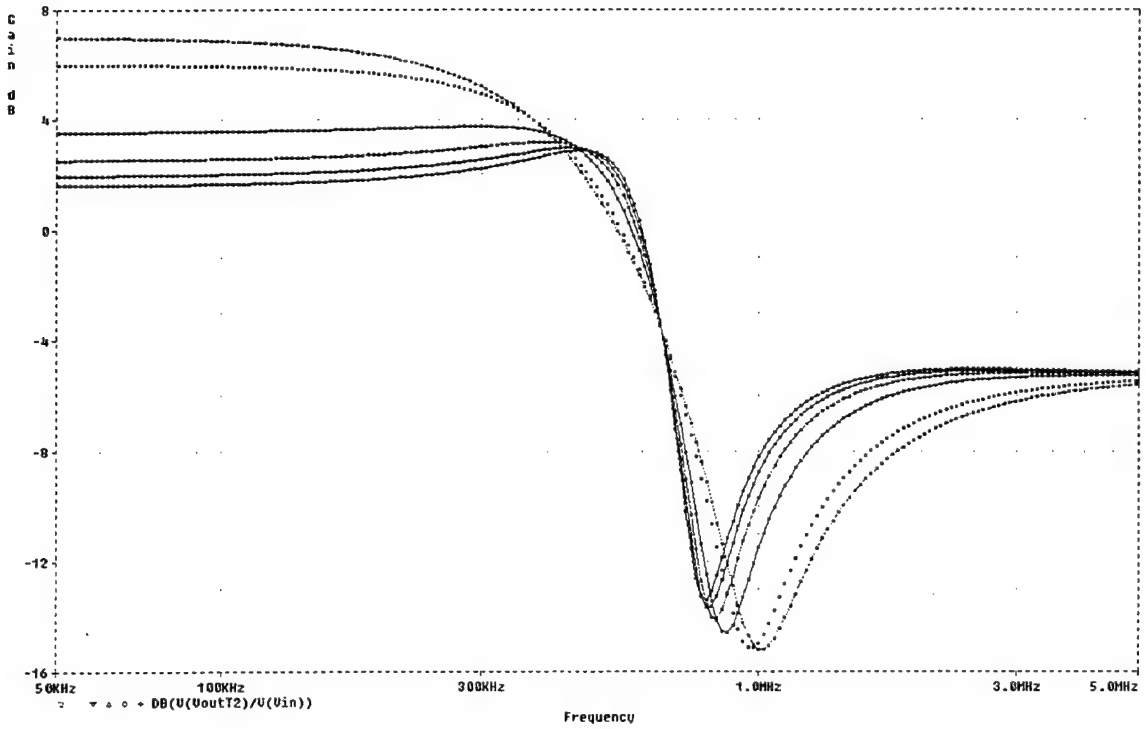
5. Notch, Quality Factor = 4, All Frequencies



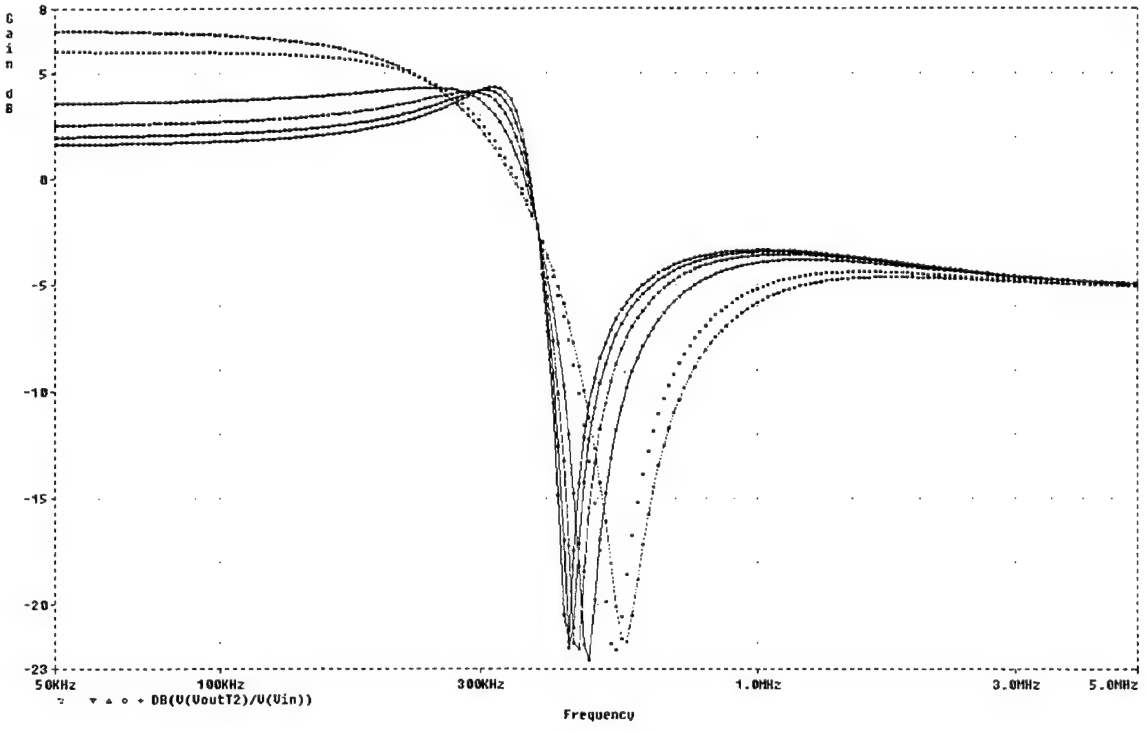
6. Notch, Quality Factor = 5, All Frequencies



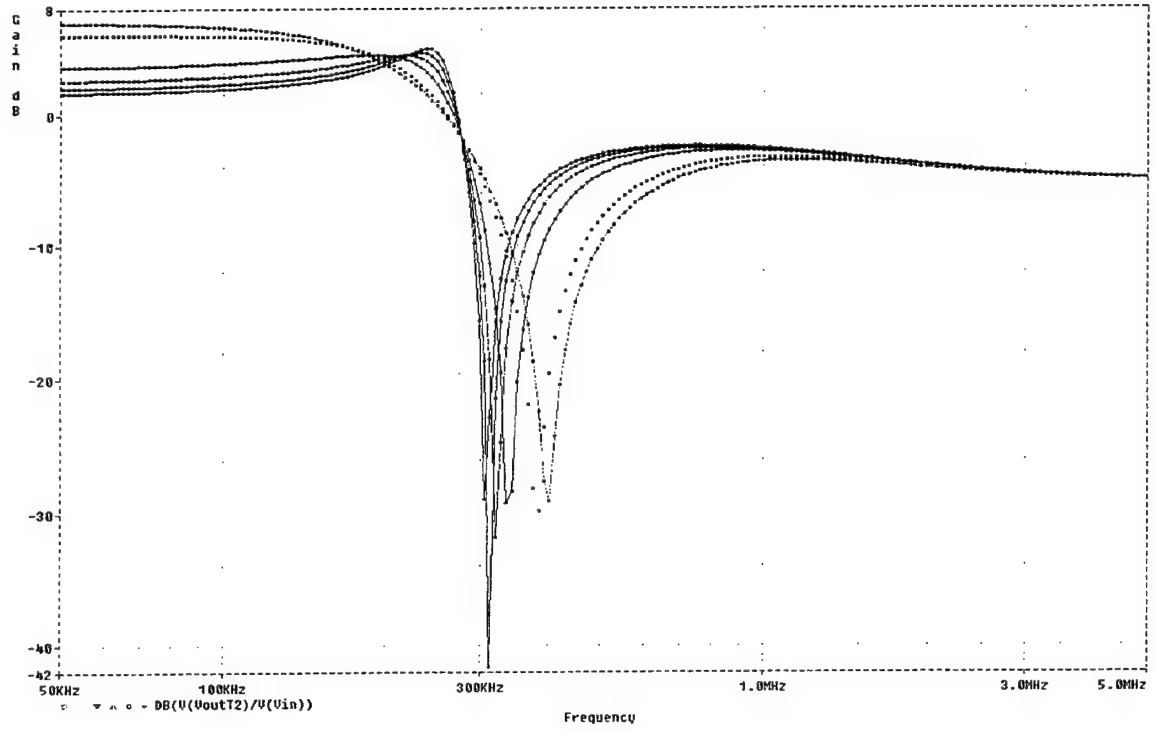
7. Notch, Frequency = 994 kHz, All Quality Factors



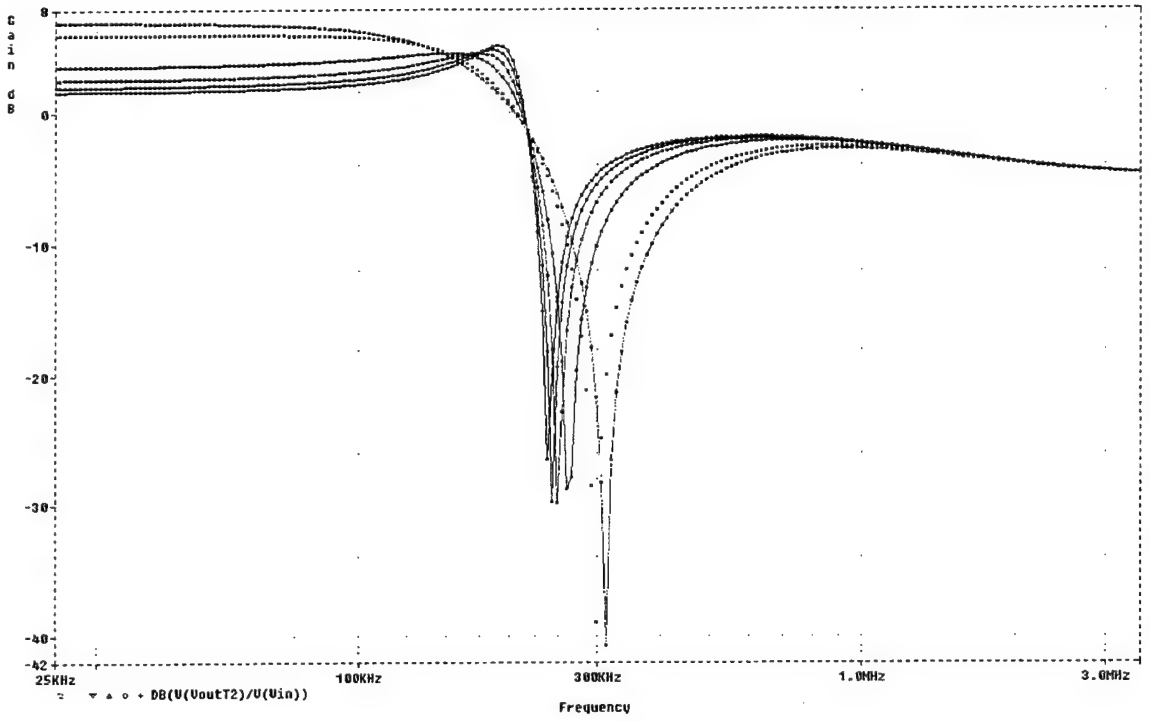
8. Notch, Frequency = 497 kHz, All Quality Factors



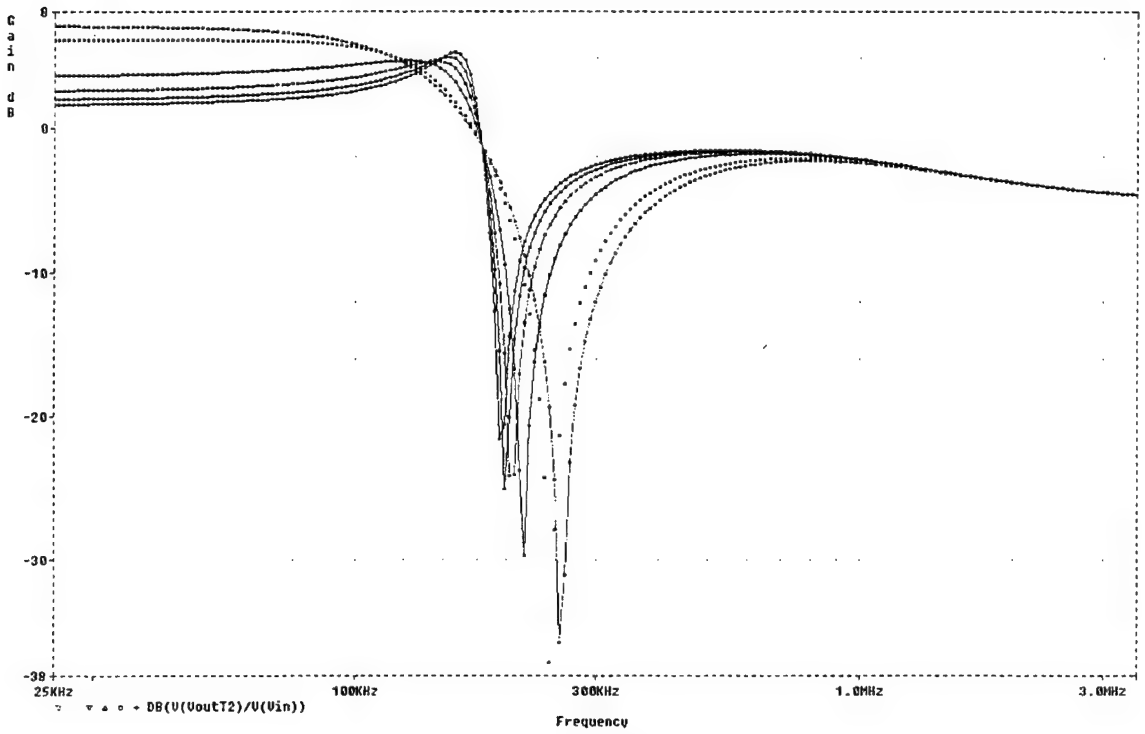
9. Notch, Frequency = 331 kHz, All Quality Factors



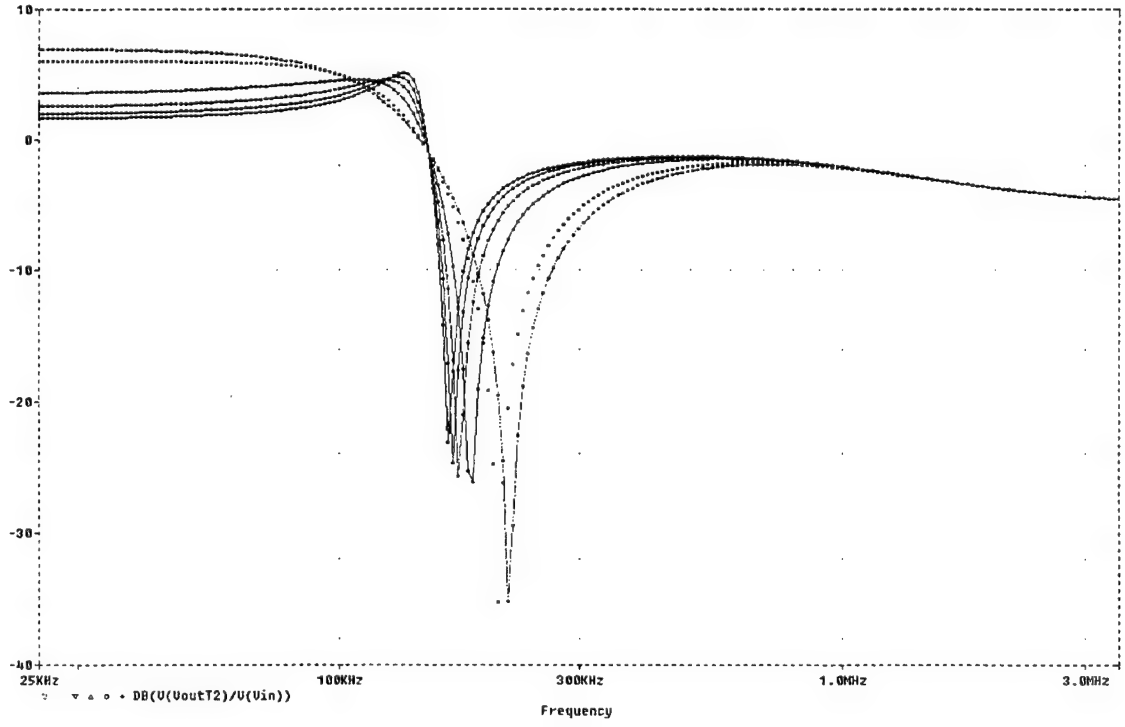
10. Notch, Frequency = 249 kHz, All Quality Factors



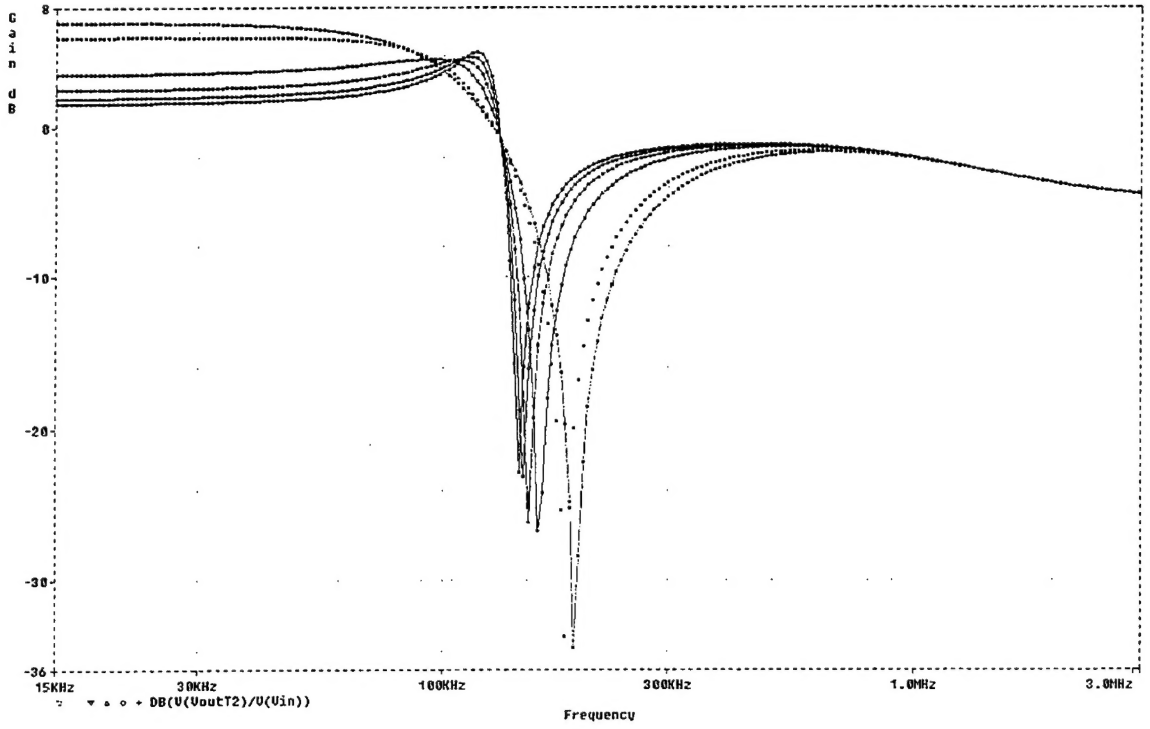
11. Notch, Frequency = 199 kHz, All Quality Factors



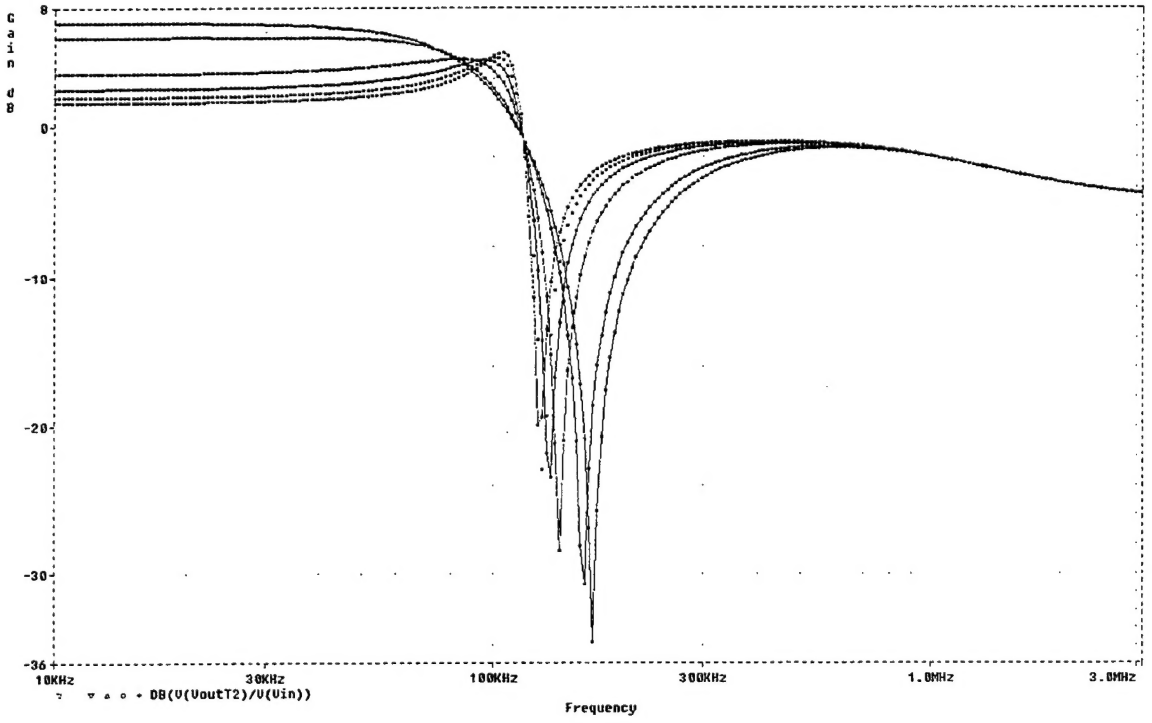
12. Notch, Frequency = 166 kHz, All Quality Factors



13. Notch, Frequency = 142 kHz, All Quality Factors



14. Notch, Frequency = 124 kHz, All Quality Factors



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